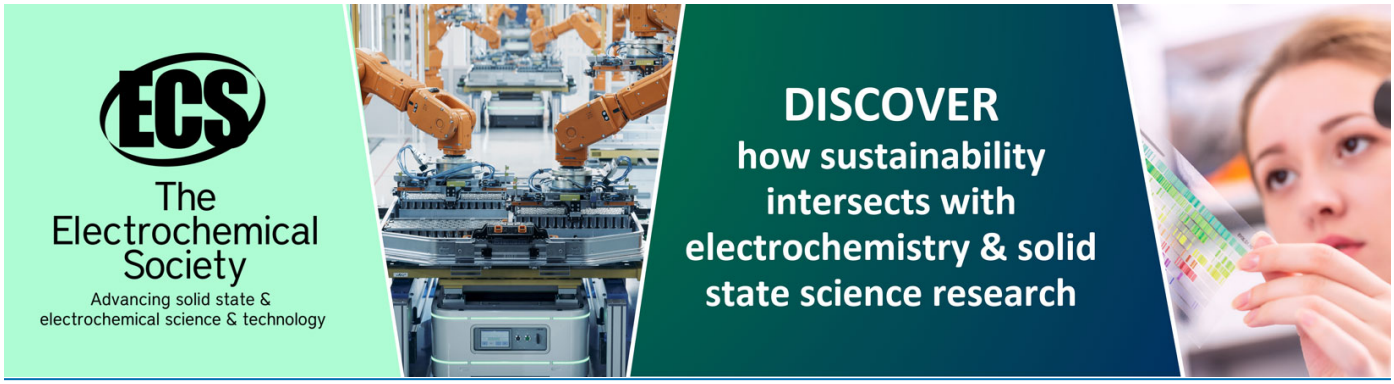
Parallel and hierarchical architectures of 4-channel MFP digitizer



IOP Conf. Series: Journal of Physics: Conf. Series **1065** (2018) 052003 doi:10.1088/1742-6596/1065/5/052003

Parallel and hierarchical architectures of 4-channel MFP digitizer

A. Angrisani[(1)], M. D'Arco[(1)], P. Monsurrò[(2)], A. Trifiletti[(2)]

[(1)]University of Naples Federico II, DIETI, Naples, Italy
[(2)]University of Rome La Sapienza, DIE, Rome, Italy

mauro.darco@unina.it; monsurro@die.uniroma1.it

Abstract. Two alternative architectures of 4-channel mixing-filtering-processing (MFP) digitizers are presented. Both architectures use four analogue-to-digital converters (ADCs), but differ in terms of layout, and are named *parallel* and *hierarchical*. Unlike conventional time-interleaved digitizers, which require ADCs characterized by relaxed sampling rate but critical bandwidth specifications, the proposed architectures are less demanding in terms of both ADCs' sampling rate and bandwidth, thus allowing less noise into the digitizer. Two digital signal processing techniques, needed to combine the digitized streams produced by the ADCs and obtain a digital representation of the input signal, are described for both parallel and hierarchical architectures. These techniques are developed on the basis of suitable error models, also discussed in the paper, and allow removing gain and aliasing errors due to analogue impairments by means of streamline calibration. The results of behavioural simulations carried out to assess the performance of the two alternative 4-channel MFP architectures are finally shown.

1. Introduction

Real-time digitizers for large-bandwidth signals need high sampling rates and large input bandwidth, in excess of 100GS/s and 50GHz, respectively, for state-of-the-art oscilloscopes. Individual ADCs cannot achieve this performance, which is obtained by means of architectures using multiple ADCs.

Several architectures use time-interleaved channels to significantly improve the overall sampling rate, but do not relax the ADCs' bandwidth specifications. Many of these use sample-and-hold amplifiers (SHAs) in the front-end of the digitizer to decouple the ADCs from the signal source. In this case, however, sufficient ADC bandwidth is still needed to cope with the abrupt variations of the SHAs' output signals.

A more effective technique, patented as digital bandwidth interleaving (DBI), uses mixers to translate the high-frequency spectral contents of the signal towards lower frequencies. The low- and high-frequency contents are then separately acquired and recombined by means of digital processing. Alternatively, the mixing, filtering, processing (MFP) architecture uses samplers or mixers to fold the signal spectrum and move high-frequency contents to lower frequencies. The superposed spectral contents are then separated by means of analogue low-pass filtering and digital signal processing operations and recombined in a digital representation of the input signal.

In this paper, two 4-channel digitizers based on MFP strategy are presented. The former solution, called *parallel* architecture, uses four parallel channels operating at one quarter of the sampling rate offered by the digitizer. The latter, more innovative, solution, called *hierarchical* architecture, uses a splitter to apply the input signal to two parallel channels, each sampling the signal at a rate equal to half the digitizer's sampling rate, and low-pass filtering the resulting waveforms. Splitting, sampling and filtering are then repeated in a second stage by bifurcating each channel into two more channels, where sampling is performed at one quarter of the sampling rate. Because the input of an MFP architecture can be reconstructed from the output samples, as shown in [1], the hierarchical 4-channel MFP structure can reconstruct the output of the first stage from the outputs of the second stage. The

advantage offered by both architectures consists in the use of less demanding hardware in terms of ADCs' sampling rate and bandwidth.

The manuscript describes the parallel and hierarchical architectures and the related error models in Section 2 and Section 3, respectively. Section 4 presents the digital signal processing required to obtain streamline calibration and signal reconstruction. Finally, Section 5 drafts simulation results for both solutions, underlining the effect of the calibration operation.

2. Parallel 4-channel MFP digitizer

The parallel architecture, shown in Figure 1, consists of 4 channels, each comprising a sampler, a low-pass filter, and an ADC. The input signal is assumed to be a Nyquist signal at a sampling rate $f_S = 1/T_S$. The sampler and ADC of channel $i \in \{0,1,2,3\}$ operate at $f_S/4$, sampling the signal at the time instants $(4n+i)T_S$, to implement time-interleaved operation. The low-pass filters have bandwidth limited to $f_S/8$, i.e. one quarter of the bandwidth of the input signal.

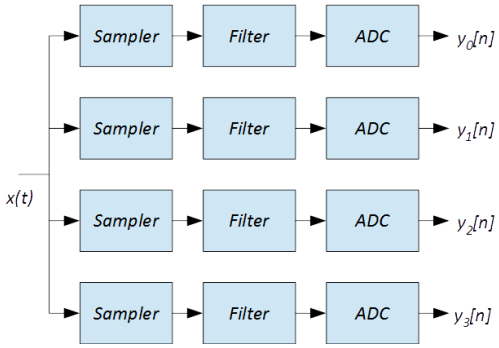


Figure 1. Block Diagram of parallel 4-channel MFP digitizer.

Samplers can be affected by gain, timing and bandwidth errors, which can be modelled by means of filters with frequency responses $F_i(f)$, $i \in \{0,1,2,3\}$, deployed in front of the respective sampler. Sampling is described as multiplication of the input signal with a pulse train. The shape of each pulse is described by $p_i(t)$, and its Fourier transform by $P_i(f)$. Filters and pulse shapes of individual channels are expected to be identical, but in practice exhibit undesired differences. The output of the filter $F_i(f)$ is named $X_i(f)$, and that of the sampler $X_{Si}(f)$; the outputs are described in the frequency domain, in the presence of input $X(f)$, by:

$$X_i(f) = F_i(f)X(f) \tag{1a}$$

$$X_{Si}(f) = \frac{f_S}{4}\sum_{k=-\infty}^{\infty} P_i\left(k\frac{f_S}{4}\right) e^{-\frac{j\pi}{2}ki} X_i\left(f - k\frac{f_S}{4}\right) \tag{1b}$$

In theory, sampling produces uncountable aliases of the input spectrum, spread along the frequency axis at a pace $f_S/4$. In practice, only a few aliases are relevant and considered in the model, because the low-pass filters remove those centered at higher frequencies. The filters have cut-off frequency $f_S/8$, and it is reasonable to assume negligible gain after $f_S/4$.

To illustrate the operating principle of the digitizer in detail, the signal bandwidth $f_S/2$ is separated in four sub-bands $\{A, B, C, D\}$. Each sub-band is further divided into positive and negative parts, labelled with subscripts letters P and N, respectively. The relevant aliases remaining after low-pass filtering are those indexed by $k = -2, -1, 0, 1, 2$. As an example, Figure 2 shows the rightward shift effect due to sampling described by k values ranging from 0 up to 3. Alias contributions undergo low-pass filtering so that only the parts within $\{-f_S/4, f_S/4\}$ are selected and forwarded to the ADCs.

The low-pass filters' frequency response $L_i(f)$, $i \in \{0,1,2,3\}$, include gain, timing error, and bandwidth mismatches between the ADCs. The outputs of the filters are:

$$X_{Fi}(f) = \frac{f_S}{4} L_i(f) \begin{pmatrix} P_{i0}X_{iAB}(f) + P_{i1}e^{-\frac{j\pi}{2}i} X_{iN}\left(f - \frac{f_S}{4}\right) + P_{i1}^* e^{\frac{j\pi}{2}i} X_{iP}\left(f + \frac{f_S}{4}\right) + \\ + P_{i2}e^{-j\pi i} X_{iCDN}\left(f - \frac{f_S}{2}\right) + P_{i2}^* e^{j\pi i} X_{iCDP}\left(f + \frac{f_S}{2}\right) \end{pmatrix} \tag{2}$$

where $P_{ik} = P_i\left(k\frac{f_S}{4}\right)$. These signals are acquired by the ADCs, clocked at time instants $(4n+i)T_S$. If the outputs of the filters are described in the digital domain, under ideal conditions it holds:

$$x_{Fi}[n] = \frac{1}{4}\left(x_A[n] + x_{BC}[n]\cos\left(\frac{\pi}{2}(n-i)\right) + \hat{x}_{BC}[n]\sin\left(\frac{\pi}{2}(n-i)\right) + x_D[n](-1)^{n-i}\right) \quad (3)$$

where $\hat{x}$ is the Hilbert transform of the time domain input signal x. In fact, for ideal samplers $F_i(f) = 1$, the Fourier transform of an ideal Dirac pulse train is a comb line spectrum with $P_{ik} = 1$ for any k, and an ideal low-pass filter with bandwidth limited to $f_S/8$ cancels all spectral contributions above the cut-off frequency.

Since the ADCs acquire at time instants $(4n + i)T_S$, their outputs in the ideal case are:

$$y[4n+i] = x_{Fi}[4n+i] = \frac{1}{4}(x_A[4n+i] + x_{BC}[4n+i] + x_D[4n+i]) = x[4n+i] \quad (4)$$

The sum (scaled by 4) of the ADC outputs is exactly the input signal sampled at time instants nT_S. Due to non-idealities, undesired terms arise: these terms can be cancelled by means of digital filtering techniques as described in Section 4.

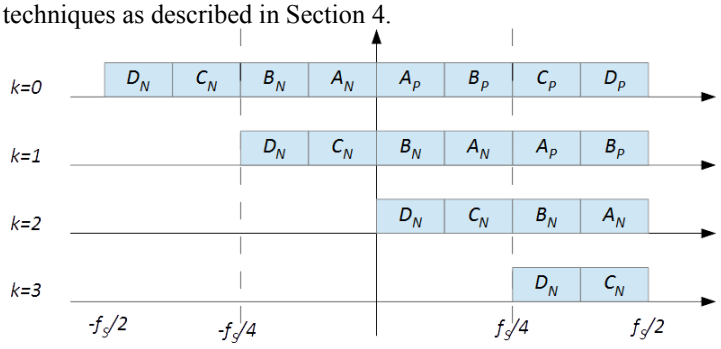


Figure 2. Effect of sampling and filtering on the spectrum of the signal: vertical dashed lines delimit the frequency interval $\{-f_S/4, f_S/4\}$.

3. Hierarchical 4-channel MFP digitizer

The layout of hierarchical 4-channel MFP is given in Figure 3, where two distinct sections can be recognized. In the first section the input signal is split to two parallel channels, where it is sampled at time instants $(2n + i)T_S$, $i = 0,1$, and low-pass filtered with cut-off $f_S/4$. In the second section each channel bifurcates into 2 parallel channels where sampling is performed at a lower rate, in time instants $(4n + 2l + i)T_S$, $l = 0,1$. The sampled versions are low-pass filtered with cut-off $f_S/8$, and finally acquired, also in time instants $(4n + 2l + i)T_S$.

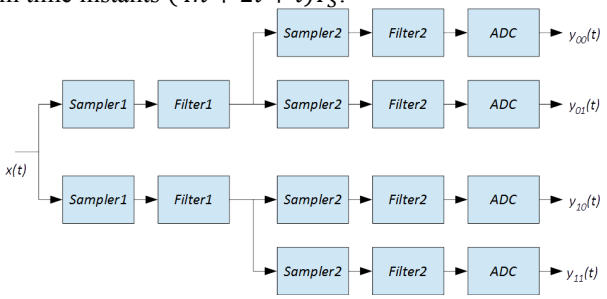


Figure 3. Block Diagram of the hierarchical 4-channel MFP digitizer

Modelling the hierarchical architecture requires defining, for both layout sections, the error filters of the samplers, $F_i(f)$ and $F_{il}(f)$, the samplers' pulse shapes $p_i(t)$ and $p_{il}(t)$, and the frequency responses of the low-pass filters $L_i(f)$ and $L_{il}(f)$, where the latter include the linear errors of the ADCs. For the first section, the following equations hold:

$$X_i(f) = X(f)F_i(f) \quad (5a)$$

$$X_{Si}(f) = \frac{f_S}{2}\sum_{k=-\infty}^{\infty} X_i\left(f - k\frac{f_S}{2}\right)P_i\left(k\frac{f_S}{2}\right)e^{-j\pi ki} \quad (5b)$$

$$X_{Fi}(f) = L_i(f)X_{Si}(f) \quad (5c)$$

Figure 4 shows the spectrum of the signal at the output of the first layout section, $X_{Fi}(f)$, hypothesizing ideal brick-wall low-pass filtering effects, which allows considering a limited set of values for *k,* namely $k = 0, \pm 1$; here the spectrum of the signal is divided in four parts, distinguished by subscript indexes $\{LL, LH, HL, HH\}$; each part includes both positive and negative frequency contents, distinguished in turn by further subscripts *P* and *N*.

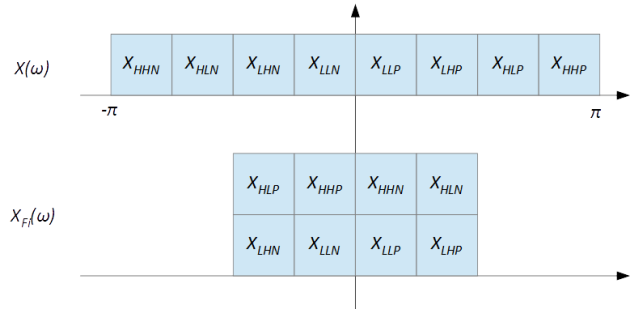


Figure 4. Spectrum of the signal at the output of the first layout section.

Similar relations hold for the second section:

$$X_{il}(f) = X_{Fi}(f)F_{il}(f) \tag{6a}$$

$$X_{Sil}(f) = \frac{f_S}{4}\sum_{k=-\infty}^{\infty} X_{il}\left(f - k\frac{f_S}{4}\right) P_{il}\left(k\frac{f_S}{4}\right) e^{-j\frac{\pi}{2}(2l+i)k} \tag{6b}$$

$$X_{Fil}(f) = L_{il}(f)X_{Sil}(f) \tag{6c}$$

Figure 5 shows the spectrum of the signal at the output of the second layout section.

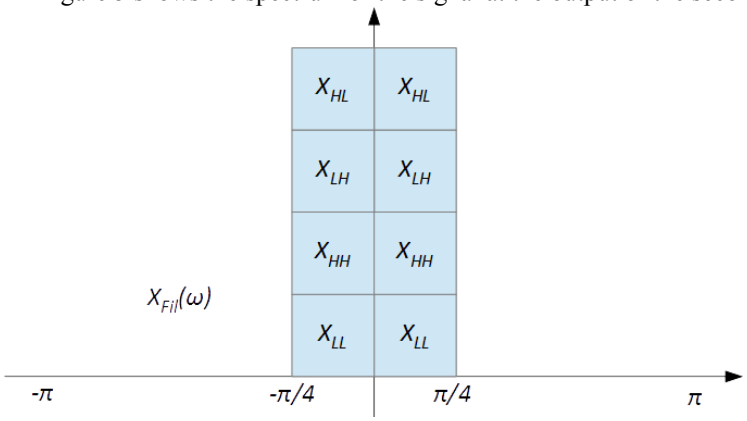


Figure 5. Spectrum of the signal at the output of the second layout section.

Noticing that $x_L = x_{LL} + x_{LH}$ and $x_H = x_{HL} + x_{HH}$, it can be shown that, under ideal conditions, the signal can be represented in the time domain as:

$$x_{Fi}[n] = \frac{1}{2}x_L[n] + \frac{1}{2}(-1)^{n-i}x_H[n] \tag{7a}$$

$$x_{Fil}[n] = \frac{1}{8}\Bigg(x_{LL}[n] + (-1)^{n-i}x_{HH}[n] + \cos\left(\frac{\pi}{2}(n-2l-i)\right)\left(x_{LH}[n] + (-1)^{n-i}x_{HL}[n]\right) + \sin\left(\frac{\pi}{2}(n-2l-i)\right)\left(\hat{x}_{LH}[n] + (-1)^{n-i}\hat{x}_{HL}[n]\right)\Bigg) \tag{7b}$$

Since the ADCs acquire the samples at time instants $(4n + 2l + i)T_S$, the digitized signal is:

$$y[4n + i + 2l] = x_{Fil}[4n + i + 2l] = x[4n + i + 2l] \tag{8}$$

Aliasing and linear filtering errors produced by non-idealities, as for the 4-channel parallel MFP digitizer, can be cancelled by means of digital signal processing operations.

4. Digital processing for error cancellation and signal reconstruction

In the presence of non-idealities, the output of both architectures is spoiled by contributions that, according to the error models given in the previous Sections, consist of terms modulated by $\cos\left(\frac{\pi}{2}n\right)$, $\sin\left(\frac{\pi}{2}n\right)$ and $(-1)^n$ functions. For instance, an input sinusoid at frequency f_1 would give rise to four output tones, at frequencies $(f_1, f_2, f_3, f_4) = \left(f_1, \frac{f_S}{4} - f_1, \frac{f_S}{4} + f_1, \frac{f_S}{2} - f_1\right)$, since multiplication by $\cos\left(\frac{\pi}{2}n\right)$ and $\sin\left(\frac{\pi}{2}n\right)$ is equivalent to frequency translation by $f_S/4$ and $-f_S/4$, and multiplication by $(-1)^n \equiv e^{j\pi n} = e^{j2\pi\frac{f_S}{2}(nT_S)}$ is equivalent to frequency translation by $f_S/2$.

It can be shown that the data streams at the output of the i-th ADC, $i = 0,1,2,3$ (the same holds for the hierarchical architecture), given an input $x[n] = \cos 2\pi f_1 nT_S$, can be represented by:

$$y_i[n] = \sum_{j=0}^{3} \mathrm{M}_{ji} \cos\left(2\pi f_j n T_S + \Psi_{ij}\right) \tag{9}$$

If the outputs of the ADCs are filtered by $H_i(f)$, and then summed, it is obtained:

$$z[n] = \sum_{i=0}^{3} y_i[n] * h_i[n] = \sum_{i=0}^{3}\sum_{j=0}^{3} \left|H_i(f_j)\right| \mathrm{M}_{ji} \cos\left(2\pi f_j n T_S + \Psi_{ij} + \angle H_i(f_j)\right) \tag{10}$$

There exists, under fairly general conditions, a set of linear equations that allows identifying the digital filters $H_i(f)$, which cancel out aliasing terms and compensate strength variations and phase displacements. In [1], the authors investigated the case of a 2-channel MFP architecture, highlighting the requirements to have a non-singular problem, and determining in closed form the solutions of the calibration problem. It can be shown that similar conditions hold for the 4-channel MFP architecture: in particular, under ideal conditions, the set of linear equations forms an orthogonal system, and for small errors the system remains non-singular. The only difference lays in the difficulties of gaining a closed-form representation of the solution, which can be however obtained numerically.

5. Simulation results

The two 4-channel MFP digitizer architectures have been simulated to investigate the effect of analogue impairments, such as non-ideal sampling pulses, gain and timing mismatches in the samplers and ADCs, and non-ideal low-pass filters. The performance in terms of linearity, before and after calibration, has been assessed, and the two architectures compared.

Also, the computational costs are evaluated, assuming a 4-channel digitizer with a sampling rate equal to 200GSps. The trade-off between accuracy and computational cost, both of which increase with the length of the correction filters, is discussed.

References

[1] L. Angrisani, M. D'Arco, P. Monsurrò, A. Trifiletti, "Multi-rate signal processing based model for high-speed digitizer," in Proc. of I2MTC2017, May 22-25, 2017, Turin, Italy.

[2] M. D'Apuzzo, M. D'Arco, 'Sampling and time-interleaving strategies to extend high speed digitizers bandwidth,' *Measurement*, 111 (2017) pp. 389-396.

[3] M. D'Apuzzo, M. D'Arco, 'A wideband DSO channel based on three time- interleaved channels', 2016 JINST 11 P08003.

[4] P. Monsurrò, and A. Trifiletti, "Calibration of time-interleaved ADCs via Hermitianity-preserving Taylor approximations," IEEE Trans. on Circuits and Sytems II, Express Briefs, vol. PP (99), pp. 1-1, 2016.