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Scaling influence on the thermal behavior of toward-THz SiGe:C HBTs

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Abstract. An extensive on-wafer experimental campaign is performed to extract the thermal resistance of state-of-the-art toward-THz silicon germanium bipolar transistors designed and developed within the European DOTFIVE project. The dependence of this critical parameter on scaling, as well as on the emitter layout, is carefully evaluated, and the resulting junction temperatures are determined.

1. Introduction

Silicon germanium (SiGe) bipolar technology is increasingly adopted in a large variety of mm-wave and near-THz applications, like high-bandwidth communications, optical transmission, medical equipments, and automotive radars. An important contribution to this trend in the European scenario has been provided by the recently-ended DOTFIVE project [1] aimed at demonstrating heterojunction bipolar transistors (HBTs) with maximum oscillation frequency f_{max}=0.5 THz [2]-[4], which the new-born DOTSEVEN [5] is expected to boost to 0.7 THz. The need for improving the performance of SiGe transistors has motivated a constant technological effort to allow aggressive lateral and vertical scaling. However, this is leading to unsustainable thermal issues induced by (i) the increase in current (and power) density, as clearly stated in a comprehensive review paper [6], and (ii) the reduction of the spacing between the intrinsic region and shallow/deep trenches filled with low thermal conductivity materials [7], for which the thermal resistances of single-finger transistors have been pushed into the thousands of K/W [8], [9].

This paper contributes to deepen the understanding of the scaling impact on the self-heating (SH) in SiGe:C HBTs by means of simple DC measurements carried out on state-of-the-art devices realized in the DOTFIVE framework.

2. Devices Under Test and Experimental Setup

Measurements were performed on about 100 single-emitter SiGe:C NPN transistors manufactured by Infineon Technologies. The devices are divided into three sets corresponding to different technology stages of the project development, which are hereinafter denoted as #1, #2, and #3. For each set, HBTs with several combinations of emitter width/length were available.

The sets are characterized by different lateral/vertical scaling levels. In particular,

- Set #2 is slightly laterally/vertically scaled compared to #1; the collector current of HBTs belonging to #2 at maximum cut-off frequency f_T is ~30% higher than that of the #1 counterparts with approximately the same emitter area.

- Set #3 transistors underwent an aggressive lateral scaling compared to #2 devices, while being vertically similar to them.

The key figures of the sets, i.e., the open-emitter breakdown voltage BV_{CBO}, the peak frequencies f_T, f_{max} at V_{CB}=0 V, and the current density J_C at peak f_T (extracted for transistors with small W_E), are reported in table 1.

Table 1. Key figures of the analyzed HBTs.

Set	BV_{CBO} [V]	peak f_T [GHz]	J_C @ peak f_T [mA/μm^2]	peak f_{max} [GHz]
#1	6.5-6.8	190	6.5-7.0	250
#2	5.2-5.9	230	9.0-9.5	310
#3	5.1-5.5	235	9.5-10	330

All the devices under test (DUTs) have single base and collector contacts (BEC configuration), as illustrated by the schematic cross-section reported in figure 1, which also evidences some key geometric parameters, like the effective emitter width W_E, the width $W_{P\text{-}poly}$ of the P^+ polysilicon window (i.e., the distance between the P^+ polysilicon edges along *x*), and the widths of the silicon boxes surrounded by deep (W_{DTbox}) and shallow (W_{STbox}) trenches. The mask (drawn) emitter width $W_{E,drawn}$ is equal to $W_{P\text{-}poly}$ for sets #1 and #2, and to $W_{P\text{-}poly}$-20 nm for set #3. Similar definitions hold for the lengths along *y*. The thicknesses (along *z*) of the shallow and deep trenches are equal to 0.3 μm and ~4.5 μm, regardless of the set.

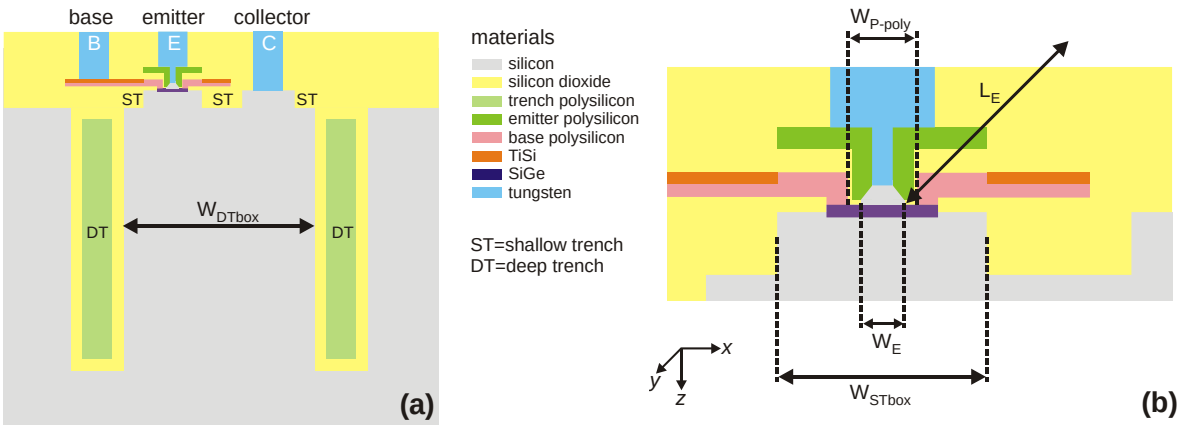

Figure 1. (a) Sketch of the cross-section of the typical HBT under test and (b) magnification of the intrinsic transistor region.

The on-wafer experimental campaign was carried out by means of a PM5 Karl Suss probe station. The electrical signals were handled by an HP4142B parameter analyzer. DC common-emitter (CE) and common-base (CB) measurements were performed by using PH100 probeheads equipped with tungsten needles. Countermeasures were taken to prevent the (sometimes destructive) oscillations that may arise under CB conditions; in particular, ferrite beads were applied to the cables in the close proximity of the DUTs. The baseplate (thermochuck) temperature T_B was set to assigned values thanks to an ATT heating/cooling system.

3. Thermal Resistance Extraction Approach

The extraction method is based on DC measurements only, and can be considered as an improved CB variant of the classic approach proposed by Dawson *et al.* [10]. The procedure is articulated in two steps, namely, (1) the calibration of the temperature coefficient of the base-emitter voltage, which is

employed as a *thermometer*, and (2) the evaluation of the slope of a CB I_E-constant V_{BE}–V_{CB} characteristic.

3.1. Transistor model

If the collector-base voltage V_{CB} is limited to values sufficiently low to neglect impact-ionization (II), the collector current can be expressed as

$$I_C = A_E \cdot J_S \cdot \exp\left(\frac{V_{BEj} + \phi \cdot \Delta T_j}{\eta \cdot V_{T0}}\right) = A_E \cdot J_S \cdot \exp\left(\frac{V_{BE} - R_{EB} \cdot I_C + \phi \cdot \Delta T_j}{\eta \cdot V_{T0}}\right) \quad (1)$$

where

- $A_E = W_E \times L_E$ [μm^2] is the effective emitter area;
- J_S [$A/\mu m^2$] is the reverse saturation current density;
- η is the ideality factor;
- V_{T0} (=25.86 mV) is the thermal voltage at ambient temperature (T_0=300 K);
- V_{BEj} and V_{BE} [V] are the internal (junction) and the externally accessible base-emitter voltages, respectively;
- $\Delta T_j = T_j - T_0$ [K] is the (average) temperature rise above ambient over the base-emitter junction;
- ϕ [V/K] is the temperature coefficient of V_{BEj} (in absolute value), i.e.,

$$\phi = -\frac{\partial V_{BEj}}{\partial T_j} \quad (2)$$

- R_{EB} [Ω] is an "aggregate" resistance dependent on the parasitic base (R_B) and emitter (R_E) resistances, as well as on the CE current gain β_F, given by

$$R_{EB} = \frac{R_B + R_E}{\beta_F} + R_E \approx \frac{R_B}{\beta_F} + R_E \quad (3)$$

3.2. Thermometer calibration

The technological coefficient ϕ was evaluated as follows. The DUTs were mounted in a CB configuration and the V_{BE}–T_B characteristics were measured at assigned I_E and V_{CB}, the values of which were chosen sufficiently low to annihilate SH, II, and resistive effects, so that $T_j \approx T_B$ and $V_{BEj} \approx V_{BE}$. As a result, the V_{BE}–T_B curve coincides with the V_{BEj}–T_j one, and ϕ can be obtained from its slope. By repeating the extraction procedure for various I_E values, it was found that ϕ logarithmically depends on I_E (almost equal to the II-free I_C), as already found for GaAs [11] and Si [12] bipolar transistors, as well as for SiGe:C devices fabricated by STMicroelectronics [8]. This dependence can be described by the following relationship:

$$\phi(I_E) = \phi_0 - \frac{k}{q} \cdot \ln\left(\frac{I_E}{A_E \cdot J_S}\right) \quad (4)$$

where k is the Boltzmann's constant and q is the elementary positive charge. Parameter ϕ_0 – an expression of which as a function of device parameters can be derived from the analysis developed in [12] – was determined by fitting (4) with the experimental ϕ vs. I_E data. It was found that ϕ_0 is set-dependent, but almost layout-insensitive for a given set; the extracted values are ϕ_0=3.53, 3.47, and 3.37 mV/K for sets #1, #2, and #3, respectively. The accuracy of the ϕ_0 estimation is witnessed by the favorable agreement at low-medium current levels between the experimental I_C–V_{BE} curves measured at various T_B for a low V_{CE} and the first-order model given by

$$I_C = A_E \cdot J_S \cdot \exp\left[\frac{V_{BE} + \phi_0 \cdot (T_B - T_0)}{\eta V_{T0} + (k/q) \cdot (T_B - T_0)}\right] \quad (5)$$

which can be obtained by substituting the logarithmic ϕ relationship (4) (with the II-free I_C in place of I_E) into the transistor model (1) and disregarding SH and resistive effects; this is shown in figure 2 for devices belonging to all sets.

From this analysis, it was also found that the scaling leads to an increase in J_S (J_S=1.7×10^{-16} A/μm^2 for set #1, J_S=2.8×10^{-16} A/μm^2 for #2, and J_S=3.1×10^{-16} A/μm^2 for #3) and a reduction in η (η=1.08-1.1 for #1, η=1.06 for #2, and η=1.035-1.055 for #3).

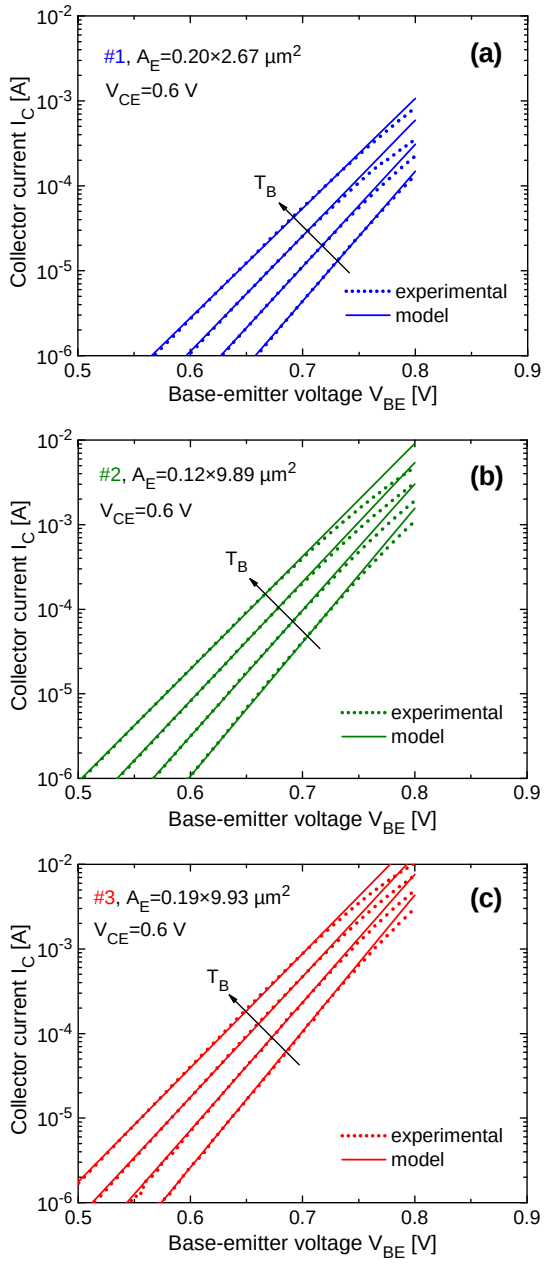

Figure 2. Collector current I_C vs. base-emitter voltage V_{BE} at V_{CE}=0.6 V and T_B=300, 320, 340, 360 K for three HBTs belonging to sets (a) #1, (b) #2, and (c) #3; experimental data (dotted lines) are compared with the calibrated model (5) (solid).

3.3. Thermal resistance evaluation

From (1), if the II-free I_C is replaced by I_E, V_{BE} can be expressed as

$$V_{BE} = R_{EB} \cdot I_E - \phi(I_E) \cdot \Delta T_j + \eta \cdot V_{T0} \cdot \ln\left(\frac{I_E}{A_E \cdot J_S}\right) \tag{6}$$

where ΔT_j is related to the dissipated power P_D by the thermal equivalent of the Ohm's law

$$\Delta T_j = R_{TH} \cdot P_D = R_{TH} \cdot (V_{BE} \cdot I_E + V_{CB} \cdot I_C) \approx R_{TH} \cdot (V_{BE} + V_{CB}) \cdot I_E \tag{7}$$

R_{TH} being the thermal resistance of the device. By substituting (7) into (6), it is found that

$$V_{BE} = \frac{1}{1+\phi(I_E)R_{TH}I_E} \cdot \left[R_{EB}I_E - \phi(I_E)R_{TH}I_E V_{CB} + \eta \cdot V_{T0} \cdot \ln\left(\frac{I_E}{A_E \cdot J_S}\right)\right] \tag{8}$$

which allows obtaining the slope γ of an I_E-constant V_{BE}–V_{CB} characteristic as

$$\gamma = \frac{dV_{BE}}{dV_{CB}} = \frac{I_E}{1+\phi(I_E)R_{TH}I_E} \cdot \left[\frac{dR_{EB}}{dV_{CB}} - \phi(I_E)R_{TH}\right] \tag{9}$$

In order to evaluate dR_{EB}/dV_{CB}, it must be considered that R_{EB} – given by (3) – depends on the junction temperature T_j through (i)

$$R_B = R_{B0} \cdot \left(\frac{T_j}{T_0}\right)^m \qquad R_E = R_{E0} \cdot \left(\frac{T_j}{T_0}\right)^m \tag{10}$$

where R_{B0} and R_{E0} are the resistance values at $T=T_0$ and *m* (>0) is a power factor assumed identical for both, and (ii)

$$\beta_F = \beta_{F0} \cdot \exp\left[\frac{\Delta E_G}{k} \cdot \left(\frac{1}{T_j} - \frac{1}{T_0}\right)\right] \tag{11}$$

where β_{F0} is the CE current gain at $T=T_0$, and ΔE_G is the difference between the bandgaps of the Si emitter and SiGe base.[1] The temperature T_j is in turn dependent upon V_{BE} and V_{CB} via (7), and therefore R_{EB} can be considered as a function of V_{BE} and V_{CB}; by differentiating,

$$dR_{EB} = \left.\frac{\partial R_{EB}}{\partial V_{BE}}\right|_{V_{CB}} dV_{BE} + \left.\frac{\partial R_{EB}}{\partial V_{CB}}\right|_{V_{BE}} dV_{CB} \tag{12}$$

from which

$$\frac{dR_{EB}}{dV_{CB}} = \left.\frac{\partial R_{EB}}{\partial V_{BE}}\right|_{V_{CB}} \frac{dV_{BE}}{dV_{CB}} + \left.\frac{\partial R_{EB}}{\partial V_{CB}}\right|_{V_{BE}} \tag{13}$$

By replacing (13) into (9), it is obtained that

$$\gamma = \frac{dV_{BE}}{dV_{CB}} = \frac{I_E}{1+\phi(I_E)R_{TH}I_E} \cdot \left[\left.\frac{\partial R_{EB}}{\partial V_{BE}}\right|_{V_{CB}} \frac{dV_{BE}}{dV_{CB}} + \left.\frac{\partial R_{EB}}{\partial V_{CB}}\right|_{V_{BE}} - \phi(I_E)R_{TH}\right] \tag{14}$$

and hence

$$\gamma = \frac{dV_{BE}}{dV_{CB}} = -\frac{\phi(I_E)R_{TH}I_E - I_E \cdot \left.\frac{\partial R_{EB}}{\partial V_{CB}}\right|_{V_{BE}}}{1+\phi(I_E)R_{TH}I_E - I_E \cdot \left.\frac{\partial R_{EB}}{\partial V_{BE}}\right|_{V_{CB}}} \tag{15}$$

After simple algebra, it can be found that

$$\left.\frac{\partial R_{EB}}{\partial V_{CB}}\right|_{V_{BE}} = \left.\frac{\partial R_{EB}}{\partial V_{BE}}\right|_{V_{CB}} = R_{TH}I_E \frac{\partial R_{EB}}{\partial T_j} \tag{16}$$

and (15) becomes

$$\gamma = \frac{dV_{BE}}{dV_{CB}} = -\frac{R_{TH}I_E \cdot \left[\phi(I_E) - I_E \cdot \frac{\partial R_{EB}}{\partial T_j}\right]}{1 + R_{TH}I_E \cdot \left[\phi(I_E) - I_E \cdot \frac{\partial R_{EB}}{\partial T_j}\right]} \tag{17}$$

[1] Equation (11) can be easily derived by reasonably assuming that the main temperature dependence of β_F comes from $(n_{iB}/n_{iE})^2$, n_{iB} and n_{iE} being the intrinsic carrier concentrations in the base and emitter, respectively.

The derivative $\partial R_{EB}/\partial T_j$ can be determined by making use of (3), (10), and (11), and is given by

$$\frac{\partial R_{EB}}{\partial T_j} = \left(\frac{T_j}{T_0}\right)^m \cdot \left[\frac{R_{B0}}{\beta_F \cdot T_j^2} \cdot \left(m \cdot T_j + \frac{\Delta E_G}{k}\right) + \frac{m \cdot R_{E0}}{T_j}\right] \tag{18}$$

It must be remarked that (18) reduces to the formula presented in [12] for Si bipolar transistors by neglecting the temperature dependence of the parasitic resistances R_E and R_B (m=0), and replacing ΔE_G with $-\Delta E_{G(BGN)}$, where $\Delta E_{G(BGN)}$ represents the difference between the bandgaps of the base and the emitter, the latter being impacted by bandgap narrowing due to the high doping level. Since $\partial R_{EB}/\partial T_j \ll 1$ for typical parameter values, $I_E \cdot \partial R_{EB}/\partial T_j$ can be neglected with respect to ϕ without loss of accuracy in (17), which reduces to [12]

$$\gamma = \frac{-R_{TH} \cdot I_E \cdot \phi(I_E)}{1 + R_{TH} \cdot I_E \cdot \phi(I_E)} \approx -R_{TH} \cdot I_E \cdot \phi(I_E) \tag{19}$$

whence

$$R_{TH} = -\frac{\gamma}{I_E \cdot \phi(I_E)} \tag{20}$$

The thermal resistance can be therefore determined by (i) measuring a V_{BE}–V_{CB} characteristic at I_E high enough to give rise to perceptible SH, the V_{CB} range being limited to values at which II can be reasonably disregarded, (ii) extracting the slope γ of this curve (see figure 3 for an example), and (iii) invoking (20), where the value of coefficient $\phi(I_E)$ is calculated from (4) for each HBT.

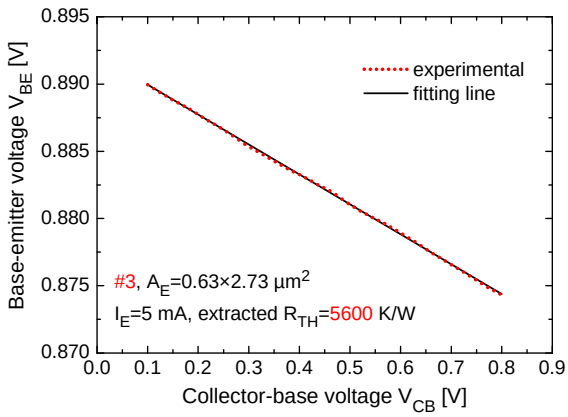

Figure 3. Extraction of the slope γ of an I_E-constant V_{BE}–V_{CB} characteristic for a device belonging to set #3.

4. Results and Discussion

Figure 4 illustrates R_{TH} as a function of effective emitter length L_E at assigned widths W_E for several HBTs belonging to all sets. It is shown that R_{TH} significantly increases by reducing L_E and can grow beyond 10^4 K/W for small areas. This confirms the findings in [8], where some CBEBC devices fabricated by STMicroelectronics were characterized by using the DC extraction technique employed in this work, and in [9], where the thermal impedances were determined by resorting to small-signal S-parameter measurements. In particular, the smallest DUTs belonging to set #1 (A_E=0.2×0.57 μm^2), #2 (A_E=0.14×0.39 μm^2), and #3 (A_E=0.11×0.63 μm^2) suffer from R_{TH}=14300 K/W, R_{TH}=21000 K/W, and R_{TH}=22000 K/W, respectively.

In figure 5, a comparison between sets is carried out for the same values of mask emitter length by varying the emitter width. The sharp R_{TH} growth for shrunk devices is apparent. It is inferred that the resistances of set #2 are slightly higher than those corresponding to #1, which can be attributed to (i) the reduced spacing between active area and shallow trench that contributes to confine the heat flow within the intrinsic transistor region, and, to a lower extent, (ii) the vertical shrinking of the heat source (i.e., the power-dissipating collector-base space charge region) induced by the smaller epi thickness and higher collector doping, which increases the volumetric power density [13]. A more

marked increment in R_{TH} is observed from set #2 to #3; this is ascribable to (i) the aggressive lateral scaling leading to a significant decrease in both W_{STbox} and W_{DTbox}, which effectively counteracts the lateral heat propagation, and (ii) the reduced cooling action of the narrowed emitter contact.

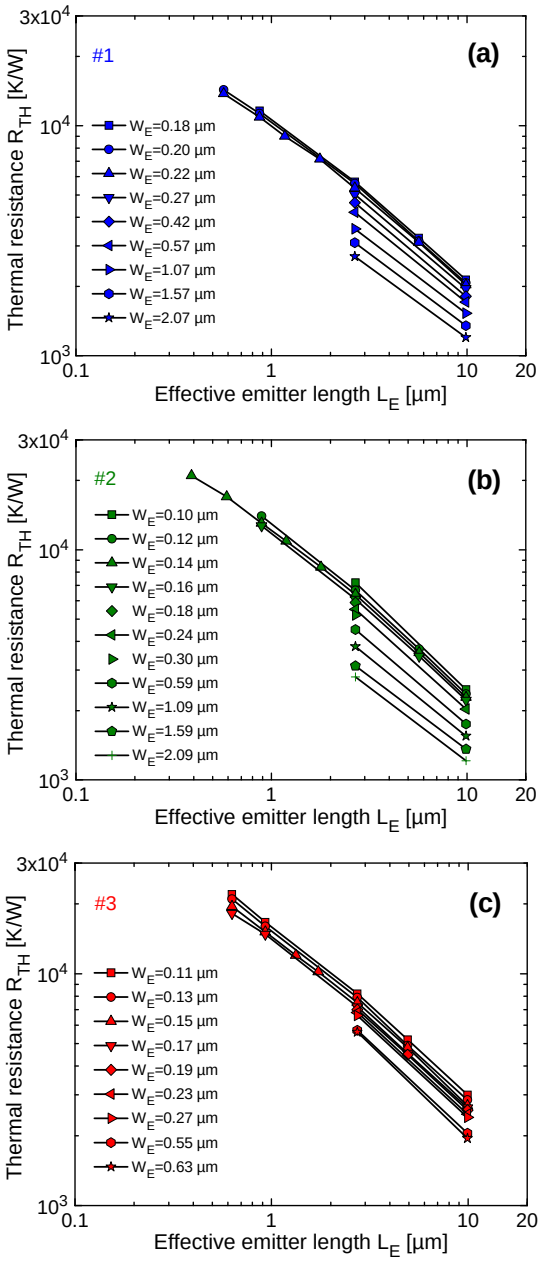

Figure 4. Thermal resistance R_{TH} as a function of effective emitter length L_E for various effective emitter widths W_E, as experimentally determined for sets (a) #1, (b) #2, and (c) #3.

It is worth noting that advanced circuits at a given technology generation are typically designed with small emitter widths. As far as the sets analyzed in this work are concerned, the best candidates are W_E=0.2 µm ($W_{E,drawn}$=0.33 µm) for set #1, W_E=0.14 µm ($W_{E,drawn}$=0.25 µm) for #2, and W_E=0.13 µm ($W_{E,drawn}$=0.2 µm) for #3. Thus, from a practical viewpoint, it is more meaningful to compare the thermal behavior of DUTs sharing such W_E values. Figure 6a shows that – with respect to set #1 – R_{TH} increases by 23.5% (#2) and 52.5% (#3) for short HBTs ($L_{E,drawn}$=0.7 µm) and by 11.2% (#2) and 39% (#3) for long ones ($L_{E,drawn}$=10 µm). Figure 6b reports the corresponding junction temperature rises ΔT_j, as determined by multiplying the thermal resistances by the power dissipated by the devices at peak f_T for V_{CE}=1 V; current density values J_C=6.8, 9, and 9.5 mA/µm^2 were reasonably

chosen as representative of sets #1, #2, and #3, respectively. It is found that the scaling-induced ΔT_j increase is almost L_E-independent, and amounts to about 15% from set #1 to #2, and to 25% from #2 to #3.

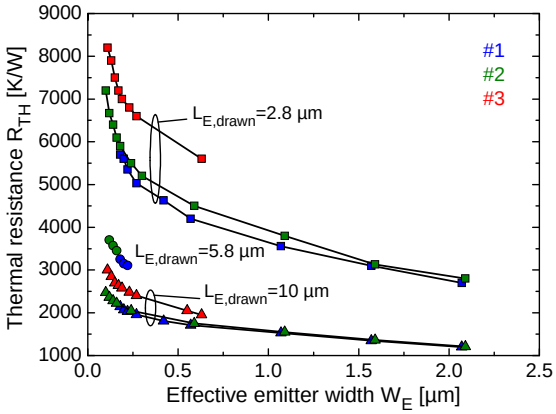

Figure 5. Thermal resistance R_{TH} as a function of effective emitter width W_E; data evaluated for the three sets under test are compared for the same values of mask (drawn) emitter length $L_{E,drawn}$.

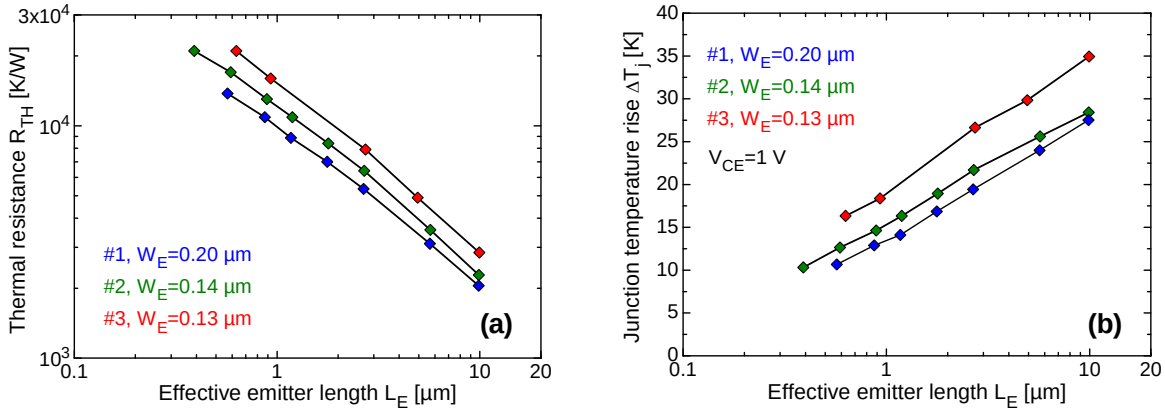

Figure 6. (a) Thermal resistance R_{TH} and (b) junction temperature rise above ambient ΔT_j as a function of effective emitter length L_E; the data correspond to the W_E values adopted for advanced circuit design.

5. Conclusions

In this paper, the influence of scaling and emitter width/length on the thermal behavior of state-of-the-art SiGe:C HBTs has been investigated through a wide experimental analysis carried out on three technology stages developed within the framework of the European DOTFIVE project. A simple extraction procedure has been exploited, which is based on DC measurements and makes use of a carefully calibrated thermometer relating the base-emitter voltage to the junction temperature at each current level. The main results can be summarized as follows: (i) small-area devices suffer from a thermal resistance R_{TH} exceeding 10^4 K/W; (ii) R_{TH} can increase by up to 50% for transistors to be employed in advanced circuits when aggressive lateral scaling is performed; (iii) the concurrent scaling-triggered growth in thermal resistance and current density leads to a significant increase in junction temperature. This study allows foreseeing that the technology improvements will paradoxically pose a serious threat to the reliability and performance of the transistors, if adequate countermeasures are not taken.

Acknowledgment
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