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Cu Pillar Low Temperature Bonding and Interconnection Technology of for 3D RF Microsystem

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Abstract. In this paper 3D interconnects technologies used Cu pillars are discussed with respect to RF microsystem. While 2.5D Si interposer and 3D packaging seem to rely to cu pillars for the coming years, RF microsystem used the heterogeneous chip such as GaAs integration with Si interposers should be at low temperature. The pillars were constituted by Cu (2 micron) -Ni (2 micron) -Cu (3 micron) -Sn (1 micron) multilayer metal and total height is 8 micron on the front-side of the wafer by using electroplating. The wafer backside Cu pillar is obtained by temporary bonding, thinning and silicon surface etching. The RF interposers are stacked by Cu-Sn eutectic bonding at 260 ℃. Analyzed the reliability of different pillar bonding structure.
   *Keywords*: Three dimension integration, Temporary bonding, Interposer.

1. Introduction

Today, the large array of vertical 3D interconnections technologies has been developed on silicon interposers to the IC chips together formed complex system. But interconnects seem to be even more diverse and complex than TSV. In 1970s the flip-chip technology has already be used for chip stacking[1], For today's applications and several supply chains are coexisting and competing to each other. The initial main driver was to increase the interconnect density to follow the integration trend. But factors like dimensions constraints, process compatibility, reliability or costs have led to the development of different technologies[2], solder Cu pillars is a major technology for many applications, it seems that Cu pillars could meet the specifications of all emerging 3D RF microsystem. We propose in this paper to discuss Cu pillars interconnects and solder bonding for 3D RF microsystem.

2. Materials and Methods

In this wafer to wafer stacking, the RF application's bandwidth limitation is directly dependent on interconnects. Copper pillars capped with tin-based solder with a pitch of 20μ m is mass production (Figure. 1). But with the coming active interposers and 3D heterogeneous stacking like GaAs packaging, the interconnect requested pillars will rapidly to shrink down to 20μ m in production this year. Strong efforts are made to reduce even more the pitch of cu pillars, but many issues remain to be solved.
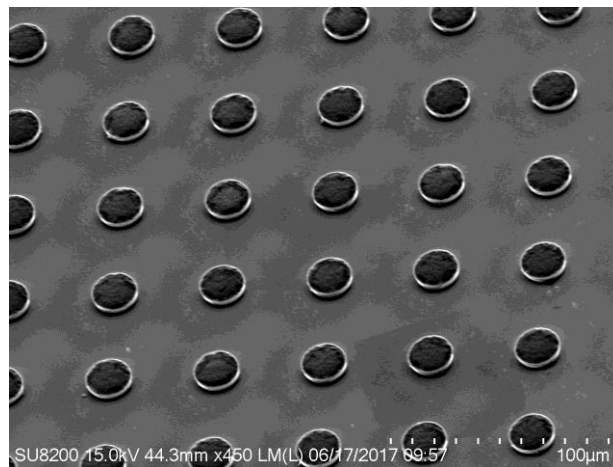
Figure 1 . Front side 20μm copper pillars by electroplating

The benefit of Cu– Sn SLID bonding for interconnects and hermetic sealing, and especially for 3D RF microsystem, is quite apparent. With interconnects or bond lines stable for large temperature variations, subsequent bonding steps, processing at elevated temperatures, or thermal annealing, for instance to activate getter materials, will not compromise the initial bonds and integrity of the package. Figure 2 shows Cu–Sn SLID bonding where Sn is placed between two Cu pillars, a pressure is applied, and the increased temperature will first cause a diffusion process between Sn and Cu to form the η -phase Cu6Sn5. Then, given enough time, the final intermetallic compound will be the stable ε -phase Cu3Sn. Since the metal layers used typically 8μ m, electroplating is used to deposit both Cu and Sn, as this offers the most economical processing[3].
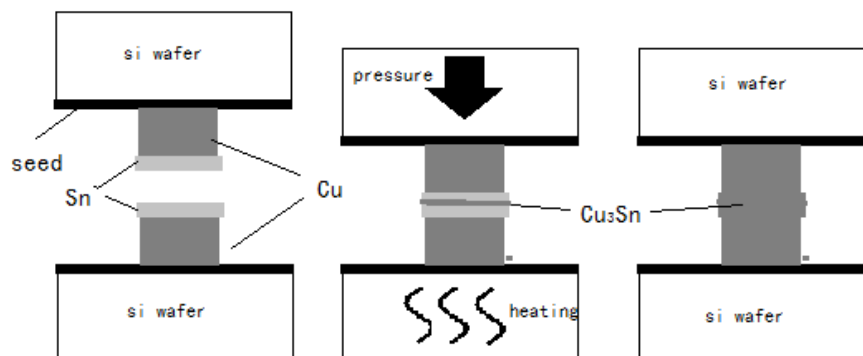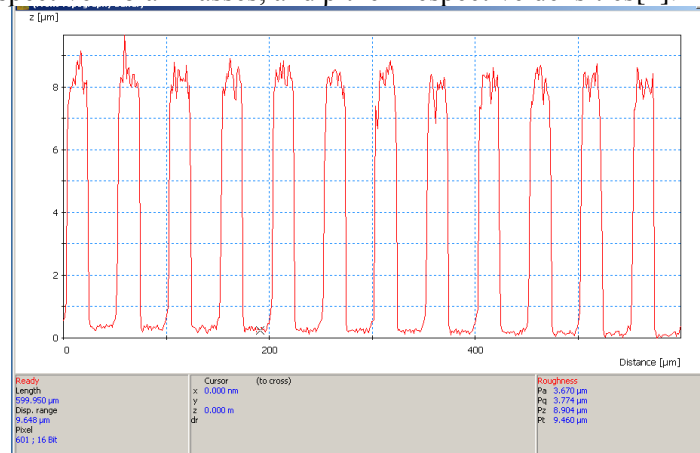

Figure 2. Cu– Sn SLID bonding

The minimum Cu/Sn thickness ratio for obtaining a steady - state Cu3Sn SLID bond, meaning that the diffusion process has come to completion, can be calculated from Eq.1 and the properties given in Table 1. Thus, the required layer thickness ratio for Cu to Sn is ⩾ 1.3. This means that for a Sn layer of 2.5 μ m, a Cu layer of a minimum thickness of 3.25 μ m is required. This amount of Cu could theoretically be the sum of the amount of Cu on both sides of the joint; however, the diffusion process may not be fully symmetric due to different temperatures of the top and bottom wafer, and because inter-diffusion will occur faster where the layers are deposited on top of each other than at the bonding interface. Thus, to ensure a sufficient amount of Cu is present in the joint, if one side as a source should be somewhat inhibited due to oxides or similar, a Cu thickness of 5μ m on each bonding partner, with a total thickness of 3μ m for Sn, Fig3 show the 8 μ m height pillars has been found to work well.

$$\frac{h_A}{h_B} = \frac{v_A}{v_B} = \frac{x}{\gamma} \frac{M_A}{\rho_A} \frac{\rho_B}{M_B} \tag{1}$$

Where h_A and h_B denote the layer thicknesses of the pure metals A and B, V their respective volumes, M their respective molar masses, and ρ their respective densities[4].


Figure 3. The 8μm height pillars

Table 1. Relevant material properties for Cu, Sn, and the corresponding intermetallic phases present in SLID bonding[4]

material	M(g)	ρ (gcm^{-3})	M/ρ	E (GPa)	R(μΩcm)	Thermal Expansion (10^{-6})	Melting Temperature e($°C$)
Cu	63.55	8.92	7.12	110	1.7	17	1084
Sn	118.71	7.28	16.31	41	11.5	23	232
Cu$_3$Sn	309.35	8.9	34.76	133	8.93	19	676
Cu$_6$Sn$_5$	974.83	8.27	117.86	117	17.5	16.3	415

3. Bonding Processes

As an alternative to using a continuous bond force, a more detailed bonding profile can take advantage of the ductile Sn layers to conform better to each other, given any nonuniformity across the wafer, compared to the significantly harder Cu surface, and the inter-diffusion process between Cu and Sn would occur with a slow temperature ramp past the melting point of Sn. Combining this with reducing the bond force at 240°C, a little above the melting temperature for Sn (232°C) [5]to account for any thermal gradients between the wafers, the reduction in bonding pressure can reduce squeeze - out of any molten Sn.   From bonding data profile where a greater temperature ramp rate to 150°C (7°Cmin^{-1}) is followed by a smaller temperature ramp rate (3°Cmin^{-1}) until reaching the melting temperature of Sn and the final soak temperature. This was done so as to reduce the amount of Sn left at the interface when reaching 240°C, and to allow for the diffusion process to occur in the bond line early in the process. The wafers were brought into contact with a bond force of 7 kN (20 MPa) after the temperature had reached 150°C. Following making of contact, the force was either reduced to 1 kN (3 MPa) at a temperature right above the melting point of Sn (240 °C)[6], or maintained high throughout the soak time.   Using this two - step temperature profile, combined with a soak time of at 10 min at 260 °C, the bond line will be fully converted to IMC, that all available Sn has been converted to Cu$_3$Sn (versus stoichiometric 25 at% Sn). The bonding result show in figure 4 .
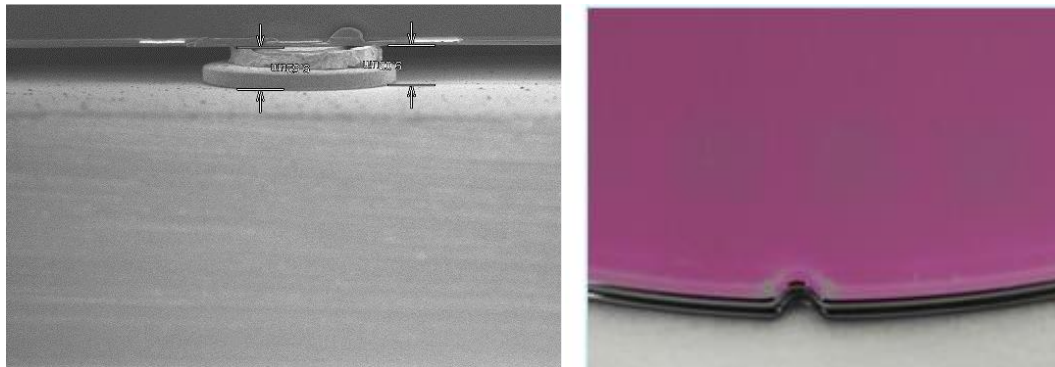
Figure 4. Pillar bonding and wafers stacking results.

The key requirements for successful SLID bonding is to remove, or convert, the oxides that are formed on the bonding surface. Both Cu and Sn oxidize, but Cu oxidation is known to be faster than Sn oxidation. Thin SnO layers can be tolerated and incorporated into the molten Sn when bonding. Therefore, the most critical oxide to remove is that of Cu prior to, and during, bonding, which can be accomplished by formic acid vapor usually requires temperatures above 100°C to be effective[7]. Note that both etching and formic acid vapor treatment are followed by a rinse step in deionized water to remove any residual compounds. To avoid a rinse step, a plasma process may be used; however, one must ensure that the temperature is kept low so as not to unintentionally melt the Sn layer. A high bonding yield is also ensured by bonding in an inert atmosphere, use of a reactive gas, or bonding in vacuum, to avoid any re-oxidation of the metal surfaces at elevated temperatures.

4. Conclusions

Since the first demonstrations of Cu–Sn SLID bonding as an excellent interconnection method for 3D RF microsystem applications, it has over recent years been demonstrated for wafer-level bonding with TSVs together with hermetic sealing and packaging at the wafer-level.

References
[1]   Munding, A. et al.   Cu/Sn solid–liquid inter-diffusion bonding, in Wafer Level 3D-ICs Process Technology, 2008 *New York. Springer Science*, 131–170.
[2]   Iino,Y. Partial transient liquid phase metals layer technique of ceramic–metal bonding. 1991 *J. Mater. Sci. Lett. New York.*10 p104 –106.
[3]   Duvall, D.S. et al. TLP bonding: a new method for joining heat resistant alloys. 1974 *Weld. J.* 53 203 –214.
[4]   Peter Ramme 2012 *Handbook of Wafer Bonding* (New York: WILEY-VCH)
[5]   Reza Ghodssi 2011 *MEMS Materials and Processes Handbook* (New York: Springer)
[6]   Rao R. Tummala 2008 *Introduction to System-on-package*   (New York: Mc Graw Hill)
[7]   John H. Lau 2010*Advanced MEMS Packaging*   (New York: WILEY-VCH)