

### **OPEN ACCESS**

# A low noise clock generator for high-resolution time-to-digital convertors

To cite this article: J. Prinzie et al 2016 JINST 11 C02038

View the article online for updates and enhancements.

# You may also like

- <u>Self-cascode and self-biased Dickson</u> <u>charge pump for fast locking wide lock</u> <u>range PLL with reduced phase noise</u> Dharani Buddha, Biswajit Jena, Chandan Kumar Pandey et al.
- <u>Research on phase-locked loop technique</u> <u>based on three-dimensional coordinate</u> <u>transformation</u> Guangjun Tan, Zhi Chen, Wei Zhao et al.
- <u>Top-down design methodology for a 2</u> ps rms Jitter at 2.56 GHz of an analog PLL based on Ring and LC Tank Oscillators E. Bechetoille, B. Joly, O. Lemaire et al.





DISCOVER how sustainability intersects with electrochemistry & solid state science research



This content was downloaded from IP address 18.225.11.98 on 08/05/2024 at 20:42

PUBLISHED BY IOP PUBLISHING FOR SISSA MEDIALAB



RECEIVED: November 15, 2015 ACCEPTED: December 23, 2015 PUBLISHED: February 12, 2016

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2015, SEPTEMBER 28<sup>TH</sup> – OCTOBER 2<sup>ND</sup>, 2015 LISBON, PORTUGAL

# A low noise clock generator for high-resolution time-to-digital convertors

J. Prinzie, a, b, c, 1 J. Christiaensen, <sup>c</sup> P. Moreira, <sup>c</sup> M. Steyaert<sup>b</sup> and P. Lerouxa, b, c

<sup>c</sup>Cern, European Center for Nuclear Research, Geneva, Switzerland

*E-mail:* Jeffrey.Prinzie@esat.kuleuven.be

ABSTRACT: A robust PLL clock generator has been designed for the harsh environment in highenergy physics applications. The PLL operates with a reference clock frequency of 40 MHz to 50 MHz and performs a multiplication by 64. An LC tank VCO with low internal phase noise can generate a frequency from 2.2 GHz up to 3.2 GHz with internal discrete bank switching. The PLL includes an automatic bank selection algorithm to correctly select the correct range of the oscillator. The PLL has been fabricated in a 65 nm CMOS technology and consumes less than 30 mW. The additive jitter of the PLL has been measured to be less than 400 fs RMS.

KEYWORDS: VLSI circuits; Analogue electronic circuits; Radiation-hard electronics; Digital electronic circuits



© CERN 2016, published under the terms of the Creative Commons Attribution 3.0 License by IOP Publishing Ltd and Sissa Medialab srl. Any further distribution of this work must maintain attribution to the author(s) and the published article's title, journal citation and DOI.

<sup>&</sup>lt;sup>a</sup>KU Leuven Departement Elektrotechniek, ESAT-ADVISE, Kleinhoefstraat 4, B-2440 Geel, Belgium

<sup>&</sup>lt;sup>b</sup>KU Leuven Departement Elektrotechniek, ESAT-MICAS, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium

<sup>&</sup>lt;sup>1</sup>Corresponding author.

# Contents

1	Introduction
2	PLL core
	2.1 Architecture
	2.2 Oscillator
3	AFC
4	Measurements
	4.1 Oscillator frequency
	4.2 Phase noise
	4.3 AFC
5	Conclusions

# 1 Introduction

High resolution time-to-digital converters (TDCs) are required in several of todays high-energy physics experiments such as CMS and ATLAS. In such applications, it is important to measure the time difference between different hit channels of the experiment with single shot precision [1, 2]rather than oversampling converters [3]. The TDCs required in those applications are typically multichannel circuits with channel counts ranging up to 64. Typically the TDCs are based on a timing generator which is a DLL locked to a high frequency reference clock [4]. In this application scope, the frequency of the DLL is targeted to run at 2.56 GHz. Since the timing resolution of the TDCs are aimed in the picosecond range (e.g. 3 ps binning), the stability of the reference clock generator of the DLL becomes critical in terms of jitter or phase noise. Ideally the DLL would receive a very clean high speed clock with no uncertainty on the clock edges. In reality there will be jitter on the clock. Since this TDC application targets LHC experiments, the circuit will use the 40 MHz reference of the accelerator that is multiplied by 64. Clock jitter will originate from both the 40 MHz external reference and internal noise generated by the components of the PLL. In the case when the jitter of the reference clock exceeds the additive jitter, generated by the PLL, it can be partially filtered by the PLL circuit. Figure 1 shows the complete architecture of the TDC in which this PLL is integrated.

1

2 2 4

4

5 5

6 7

8



Figure 1. TDC architecture.

# 2 PLL core

#### 2.1 Architecture

Figure 2 shows the overall architecture of the PLL. In this design, a traditional charge-pump and phase-frequency detector (PFD) is used to control the PLL. The core of the PLL uses a low noise LC-tank based VCO. The PLL has been designed to allow full customization of all blocks in terms of bias settings. Typically all bias currents can be programmed to be 0.1 up to 3 times the nominal value. In this way, the bandwidth and the noise of the PLL can be configured to match individual user needs for different applications. The phase-frequency detector of the PLL consists of two custom D-type flip flops that have an automatic load 1 and asynchronous reset [5]. A high speed cell is used to reduce the risk of dead zone of the detector and reduce the minimal delay that is required in the feedback path of the PFD. Finally a pseudo differential signal is generated from the single-ended PFD outputs to drive the charge pump switches. It is essential that the UP and DOWN signals at the charge pump are in phase. The buffer from the PFD to the charge pump therefore includes regenerative latches to align the phase during inversion.

Figure 3a shows the simplified schematic of the charge pump. In this figure, the switches that control the charge pump are represented by MOS devices. In reality, transmission gate switches are used to prevent charge injection from the channel of the devices. The transmission gates were designed with equal gate capacitances such that the charge is equal in both P- and N-type devices. As shown on figure 3a, the charge pump has two branches. When the current is switched to the output, the top current is only switched from the left branch to the right branch. In this way, the current source does not have to switch on since it is kept turned on when the charge pump is inactive. This prevents the drain nodes of the charge pump from going to the power or ground rails. This would result in severe charge sharing when the UP or DOWN signals go high. An opamp is used in-between the loop control voltage and the replica branch of the charge pump to ensure that both voltages are identical. It is essential that this opamp can operate nearly rail-to-rail since the control



Figure 2. PLL architecture.

voltage of the PLL can also go rail-to-rail. A gain of 30 is used in the opamp with a bandwidth of 1 MHz. This bandwidth can be low since this is only a reference path. Note that the input of the opamp does not directly use the control signal of the PLL but the voltage across main the capacitor of the loop. This voltage is much more stable since there is no periodic transient across it as is the case with the loop resistor.

A 6-bit DAC is used to set the current of the charge pump to control the loop gain and thus the bandwidth of the PLL. In both P- and N-MOS side bias points, large decoupling capacitors to ground and supply are added to prevent complete bias disturbance when single-event strikes occur on the bias nodes. A 5 bit controllable resistor is added to the PLL loop to control the damping of the loop since the PLL requires a zero in the loop for stability as is shown in figure 3b. The resistor can be programmed in combination with the charge pump current to select the required bandwidth and damping of the PLL. The divider of the VCO is a 2 stage divider since the standard logic in 65 nm process cannot run at 3.2 GHz (maximum frequency) in the worst corner. A custom high speed CML prescaler is included. In the first stage a divide by 4 is performed using two sequential CML dividers. Since these circuits consume 2 mA of current, they are less sensitive to SEU effects due to the high bias currents and only 2 LSBs of the counter are calculated here. Therefore no triplication is included. A second stage includes a divide-by 16 that uses standard cells. This divider is much



Figure 3. a) Charge pump schematic b) Programmable loop resistor.

more sensitive to SEUs since small devices are used and MSBs are calculated in this stage. An SEU in this stage would result in a severe transient of the PLL. Therefore triple-modular redundancy is included in this part.

#### 2.2 Oscillator

The oscillator has been designed for low phase noise. Since the phase noise of the PLL depends on the tank, this has been optimized to be as low as possible for the given power consumption. To improve the phase noise of the oscillator, a smaller inductor can be chosen with a larger capacitor. At this frequency range, the Q-factor of the inductor is much worse than the Q-factor of the varactors or capacitors. Reducing the inductance also reduces the series resistance of the tank and thus the phase noise. However larger Gm cells that consume more power are necessary to ensure the swing of the oscillator. An optimal inductor of 700 pH is used with a current of 5 mA.



Figure 4. a) Oscillator implementation b) Discrete capacitor banks c) Virtual ground.

Figure 4a shows the oscillator circuit. A PMOS current source is used to reduce the close-in 1/f noise since PMOS devices intrinsically have lower 1/f noise. To increase the tuning range of the VCO, discrete controllable capacitors are added to the tank to extend the control range of the varactor. The varactors are implemented with N-type MOSCAP devices. In normal operation, the capacitors are preset and the PLL is controlled with the varactors. However another frequency band can be selected with different capacitors. These capacitors are all equal in size and the capacitance is selected such that there is more than half of the tuning range of the varactor overlap between different bands to ensure that there are no dead bands. Figure 4b show a detailed circuit of the switching method of the capacitors. The bottom switches are small and are just used to bias the middle transistor when switched on. The middle switch is an N-MOS transistor with large size to reduce the on resistance that limits the Q of the capacitor banks. Placing the transistor in-between the nodes improves the Q factor by 2 since a virtual ground is created as is shown in figure 4c. This improves the phase noise and power consumption of the oscillator.

### 3 AFC

The discrete capacitors of the oscillator are implemented with MOMCAPs, they have a very good Q factor compared to MOSCAP varactors but suffer from large variability on different process corners. The result is that the frequency bands shift on different corners. The variations can be



Figure 5. AFC system architecture.

so large that the correct preset of the banks cannot be guaranteed in advance such that the PLL can never lock. Therefore an automatic frequency calibration algorithm is included in this chip. During startup, the automatic frequency calibration (AFC) algorithm is launched and the correct setting of the VCO is calculated. Later, this algorithm does not run anymore. The logic however is synthesized to include triple modular redundancy and all registers are continuously clocked to prevent the calculated values from being lost after an SEU hit.

Figure 5 shows the system components of the AFC. During calibration, the PLL is stopped and the oscillator is free running with a constant voltage. Two counters are reset and start running. One counts on the reference clock where the other counts the divided oscillator. Depending on the preset value of the oscillator and the frequency of the reference clock, either the first or the second counter will timeout first. A binary search algorithm updates the preset value of the oscillator based on which timer was first completed and the counters are reset and ran again. For each bit (4 bits in this design), there has to be a count and an update of the bits. Thus the calibration time is constant and mainly determined by the counter depth. Careful synchronization has been implemented in the counters since the VCO clock is asynchronous to the clock of the FSM. Both counters count asynchronously to the FSM but the timeout-flags and reset events are synchronized to the FSM. The counters are designed as sequential ripple counters where each stage is triplicated for SEUs. The FSM uses traditional TMR.

# 4 Measurements

#### 4.1 Oscillator frequency

In the prototype chip the PLL could be put into open loop to measure the frequency and phase noise performance of the oscillator individually. Figure 6a and figure 6b show the oscillation frequency of the oscillator for all different operating points of the VCO. Figure 6a shows the change in oscillation frequency for varying control voltages at the input. The different bands are shown where extra discrete capacitors are added. Since the AFC algorithm can be overwritten with pre-defined values, all bands can be measured individually. As can be seen from figure 6a, there is an overlap of more than 2/3 between all bands. This has been done to make sure that there is no empty zone between the bands. An advantage of this large overlap is that the control voltage of the VCO is relatively



Figure 6. a) Oscillation frequency vs. Vc b) Oscillation frequency vs. digital tuning caps.

constrained within a small voltage range around VDD/2 which results in a good output impedance of the charge-pump. Figure 6b shows the frequency shift when extra capacitors are added to the VCO for 0 V, 0.6 V and 1.2 V control voltages where 1.2 V corresponds to the highest frequency. The error bars show the variation in frequency measured for 5 different chips. As is clear from the plot, this variation is relatively small. However these measurements were performed on chips that are processed on the same wafer and thus only inter-die mismatch from the same batch is concerned here.

The supply sensitivity of the VCO has been measured by changing the supply voltage and measuring the change in oscillation frequency. The supply sensitivity of the oscillator was measured to be 24 MHz/V. The supply sensitivity is the worst at the center of the control voltage since the gain of the VCO is the largest at that point with a value of 240 MHz/V.

#### 4.2 Phase noise

To measure the phase noise of the closed-loop PLL, extra circuitry was added to the prototype chip to inject a very clean reference clock to the chip. Since typical bit-pattern generators have internal jitter of several picoseconds, this equipment cannot be used and RF test equipment has to be used to conduct the tests. An ultra-low phase noise sine-wave generator is used as reference clock of the PLL, since a 40 MHz signal has low slew rates, large amounts of jitter are added at the input stage



Figure 7. Phase noise measurement setup.



Figure 8. a) Phase noise measurement b) Jitter histogram.

of the chip, therefore a 640 MHz sine wave is injected and an on-chip divider divides the clock to 40 MHz to feed the PLL as shown in figure 7. In this way, a low jitter input clock (< 200 fs RMS) can be inserted. All of the following measurements include this phase noise and cannot be omitted.

Figure 8a shows the phase noise measurements of the open-loop VCO and closed loop PLL. As is shown on the plot, the phase noise of the PLL at high offset frequencies is dominated by the phase noise of the VCO. A slight increase around the bandwidth of the PLL is observed due to the thermal noise of the loop resistor of the PLL. The phase noise of the VCO is measured to be -124 dBc/Hz at 1 MHz offset frequency at a center frequency of 2.56 GHz with a power consumption of 6 mW. The integrated phase noise of this measurement is 400 fs rms with a power consumption of 30 mW. A second noise measurement has been performed with a digital sampling oscilloscope (Tektronix DPO 7000). The measurements are triggered on the output data and a large frame of the data is captured. During post processing, the time difference to an ideal clock, which has a period equal to the average period of this window, is calculated and plotted in figure 8b. The total jitter was measured as 526 fs. Since the internal timebase of the scope has a jitter of 200 fs, this can be quadratically subtracted from our measurement since the noise is uncorrelated. This measurement then shows a total rms jitter of 486 fs which is comparable to the phase noise measurements.

#### 4.3 AFC

Figure 9a shows the flow of the AFC algorithm. A 40 MHz reference clock is used, which corresponds to a period of 25 ns. A sampling scope is triggered upon the start of the AFC. An extra IO pin is added to the prototype chip to indicate that the AFC is busy. This plot shows the post-processed data of the instantaneous period and frequency of the waveform. Before the start, the PLL was already in lock but the AFC was restarted. As shown in figure 9a, the AFC algorithm conducts a binary search in 4 steps where in each step, the frequency gets closer to the reference clock frequency. After the 4 steps, the control is handed over to the PLL and there is some small re-acquisition depending on the actual phase difference and voltage states of the PLL. The total calibration time is  $100 \,\mu$ s with an additional acquisition time of  $3 \,\mu$ s.



Figure 9. AFC cycle measurement.

# 5 Conclusions

In this work a low noise PLL is presented to convert a 40 MHz reference clock to 2.56 GHz clock for high resolution TDC applications. The PLL is based on a low phase noise LC tank oscillator and has an internal additive jitter of only 400 fs. The core circuit has a power consumption of only 30 mW with a programmable bandwidth from 400 kHz to 3 MHz. An automatic frequency calibration algorithm is included to select the correct band of the VCO depending on the reference frequency and process variations. The prototype has been fabricated in a 65 nm CMOS technology. A die photograph is shown in figure 9b.

### References

- L. Perktold and J. Christiansen, A Flexible 5 ps Bin-Width Timing Core for Next Generation High-Energy-Physics Time-to-Digital Converter Applications, in The 8th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), Aachen, Germany, 12–15 June 2012, pg. 179–182.
- [2] S. Henzler, S. Koeppe, W. Kamp, H. Mulatz and D. Schmitt-Landsiedel, 90nm 4.7ps-Resolution 0.7-LSB Single-Shot Precision and 19pJ-per-Shot Local Passive Interpolation Time-to-Digital Converter with On-Chip Characterization, IEEE ISSCC Dig. Tech. Papers (2008) 548.
- [3] Y. Cao, W. De Cock, M. Steyaert and P. Leroux, *1-1-1 MASH Time-to-Digital Converters With 6 ps Resolution and Third-Order Noise-Shaping*, *IEEE J. Solid-State Circuits* **47** (2012) 2093.
- [4] J. Prinzie, M. Steyaert and P. Leroux, A single shot TDC with 4.8 ps resolution in 40 nm CMOS for high energy physics applications, 2015 JINST 10 C01031.
- [5] A. Homayoun and B. Razavi, Analysis of Phase Noise in Phase/Frequency Detectors, IEEE Trans. Circuits Syst. I 60 (2013) 529.