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High-Performance P-Channel Diamond Metal–Oxide–Semiconductor Field-Effect Transistors on H-Terminated (111) Surface

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Through the enhancement of hole accumulated density near hydrogen-terminated (111) diamond surfaces, low sheet resistance ($\sim 5 \text{ k}\Omega/\text{sq}$) has been obtained compared with widely used (001) diamond surfaces ($\sim 10 \text{ k}\Omega/\text{sq}$). Using the hole accumulation layer channel, a high drain current density of -850 mA/mm was obtained in p-channel metal–oxide–semiconductor field-effect transistors (MOSFETs). This drain current density is the highest value for diamond FETs. The high drain current on the (111) surface is attributed to two factors: The low source and drain resistances owing to the high hole carrier density and the high channel mobility at a high gate–source voltage on the (111) surface.

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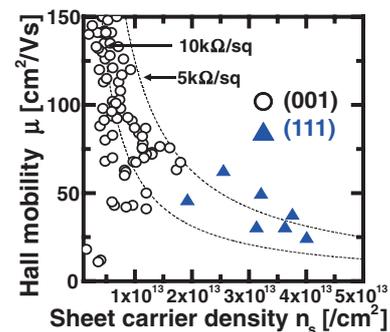
Radio-frequency (RF) diamond FETs have already been realized using hole accumulation layer channels on hydrogen-terminated (H-terminated) diamond surfaces.^{1,2)} To date, a maximum drain current (I_{DSmax}) of -350 mA/mm and cut-off frequency (f_{T}) of 30 GHz have been achieved on H-terminated (001) diamond films.^{3–5)} Much higher I_{DSmax} of -790 mA/mm and f_{T} of 45 GHz have recently been reported on (110)-preferred large-grain diamond films although there are many grain boundaries.^{6,7)} This is because the H-terminated (110) diamond surface shows lower sheet resistance than H-terminated (001) films.⁷⁾ However, the H-terminated (110) surface is not smooth enough to allow excellent FET operation.

Here, we focus on (111) diamond surface where much better homoepitaxial growth can be obtained compared with (110) surface, but FET fabrication is still very limited.⁸⁾ On the (111) surface, good transistor performance has been obtained on diamond metal–oxide–semiconductor field-effect transistors (MOSFETs). In addition, we discuss the reasons for the superiority of the (111) surface compared with the (001) surface.

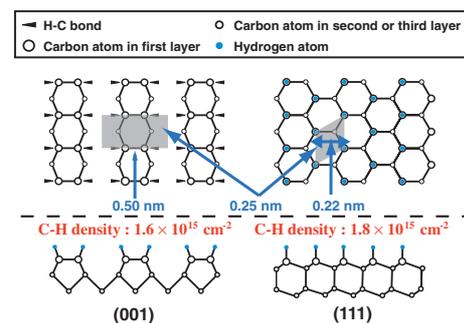
First, to compare the hole accumulation layer on H-terminated (111) and (001) diamond surfaces, we used IIa-type (111) diamond substrates and homoepitaxial films grown on Ib-type (001) substrates. H-termination was achieved by hydrogen plasma. Before the H-termination process, both substrates were polished using a polishing scaife. The root mean square (RMS) values of the surface roughness for H-terminated (001) and (111) diamond substrates are ~ 0.5 and ~ 0.7 nm, respectively.

Then, we fabricated p-channel diamond MOSFETs on the H-terminated (111) surface by the self-alignment gate lift-off technique.⁵⁾ The gate width was $50 \mu\text{m}$. To evaluate the gate length dependence of I_{DSmax} , we changed the gate length from 0.3 to $1 \mu\text{m}$. The actual gate lengths are almost the same as the designed lengths. Even in the $0.3\text{-}\mu\text{m}$ -gate-length MOSFETs, the actual gate lengths were $0.3 \pm 0.05 \mu\text{m}$ and therefore, the fluctuation in the actual gate length is small.

The hole accumulation layer on H-terminated (111) surfaces has a sheet carrier density (n_{s}) of over $2 \times 10^{13} \text{ cm}^{-2}$, which is more than double that of (001) surfaces [Fig. 1(a)]. The sheet resistance on (111) surfaces is



(a)



(b)

Fig. 1. (a) Hall measurement results of hole accumulation layer on H-terminated (001) and (111) diamond surfaces. (b) Schematic top and side views of H-terminated (001) and (111) surfaces. The H–C bond densities of (001) and (111) surfaces are 1.6×10^{15} and $1.8 \times 10^{15} \text{ cm}^{-2}$, respectively.

distributed around $5 \text{ k}\Omega/\text{sq}$, which is about half that on (001) surfaces.

The high sheet carrier density on (111) surfaces is caused by the high H–C dipole charge density. Although the origin of the hole accumulation layer remains to be determined, we proposed that negative fixed charges by adsorbates on $\text{H}^{+\delta}\text{--C}^{-\delta}$ dipoles of H-terminated diamond surfaces are essential to induce high-density hole carriers.⁷⁾ The H–C bonds act as electric dipoles owing to the difference in the electronegativities of H (2.1) and C atoms (2.5). The positively charged side, $\text{H}^{+\delta}$, attracts negatively charged adsorbates and positively charged carriers (holes) emerge on the semiconductor side to satisfy charge neutrality. Because of small RMS values of the (111) and (001) surfaces, both surfaces are flat enough to consider their H–C dipole effects on each surface. On flat (111) and (001) surfaces, H–C dipole densities are

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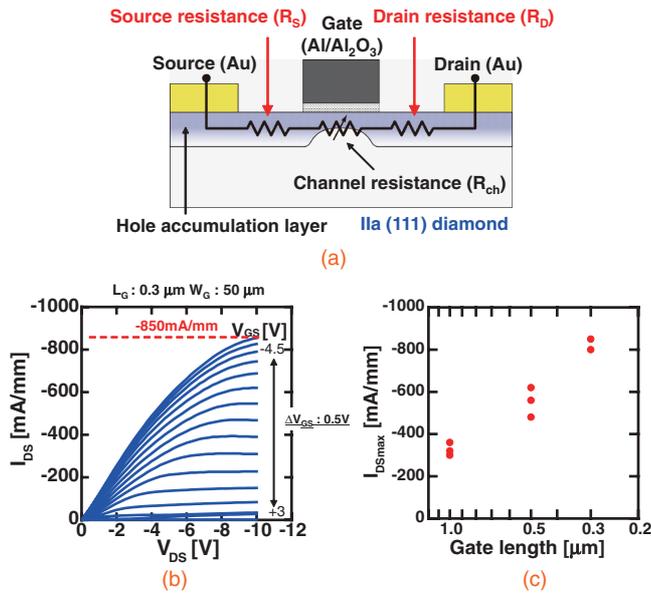


Fig. 2. (a) Schematic cross section of diamond MOSFET on 111 diamond film. (b) $I_{DS}-V_{DS}$ characteristics of 0.3- μm -gate-length diamond MOSFET on the (111) surface. (c) Gate length dependence of $I_{DS\text{max}}$ on the (111) surface.

1.8×10^{15} and $1.6 \times 10^{15} \text{ cm}^{-2}$, and the H-C angles from each surface are 90° and 71° , respectively [Fig. 1(b)]. In the H-C dipole, a charge of -0.05 to $-0.10e$ (where e is the elementary charge) can be transferred from each hydrogen atom to each carbon atom. Then, the calculated carrier densities from the dipole charge density are 9.0×10^{13} and $7.5 \times 10^{13} \text{ cm}^{-2}$, respectively. The calculated carrier density on the (111) surface is higher than that on the (001) surface, similar to Hall effect measurements in Fig. 1(a).

Because the diamond MOSFETs were fabricated by the self-alignment gate lift-off technique, the gate-source and gate-drain spacings are the same and therefore, the parasitic source resistance (R_S) is equal to the drain resistance (R_D) [Fig. 2(a)]. For the diamond MOSFETs fabricated, the gate-source and gate-drain spacings are both $0.3 \mu\text{m}$, which is comparable to the gate length. Therefore, R_S and R_D are not negligible in the total resistance.

The $0.3\text{-}\mu\text{m}$ -gate-length diamond MOSFET fabricated on H-terminated (111) surface exhibited $I_{DS}-V_{DS}$ characteristics with excellent current saturation and pinch-off characteristics. The $I_{DS\text{max}}$ and transconductance (g_m) are -850 mA/mm and 160 mS/mm , respectively [Fig. 2(b)]. This $I_{DS\text{max}}$ is the highest value for diamond FETs. Figure 3(c) shows the gate length dependence of $I_{DS\text{max}}$. Higher $I_{DS\text{max}}$ was obtained in MOSFETs with shorter gate lengths. Although there is fluctuation in $I_{DS\text{max}}$ in Fig. 3(c), $I_{DS\text{max}}$ of the $1\text{-}\mu\text{m}$ -gate-length MOSFET on the (111) surface was -350 mA/mm , which is comparable to those of the best (001) diamond FETs obtained by three independent groups.³⁻⁵ Those gate widths are $50\text{--}100 \mu\text{m}$, which is almost the same as that of (111) diamond MOSFETs in this work. These results indicate that the diamond surface orientation has the strong influence on $I_{DS\text{max}}$ in diamond FETs. f_T and maximum oscillation frequency (f_{max}) were 22 and 25 GHz , respectively.

One of the reasons for the high $I_{DS\text{max}}$ of -850 mA/mm is the low sheet resistance on the H-terminated (111) surface.

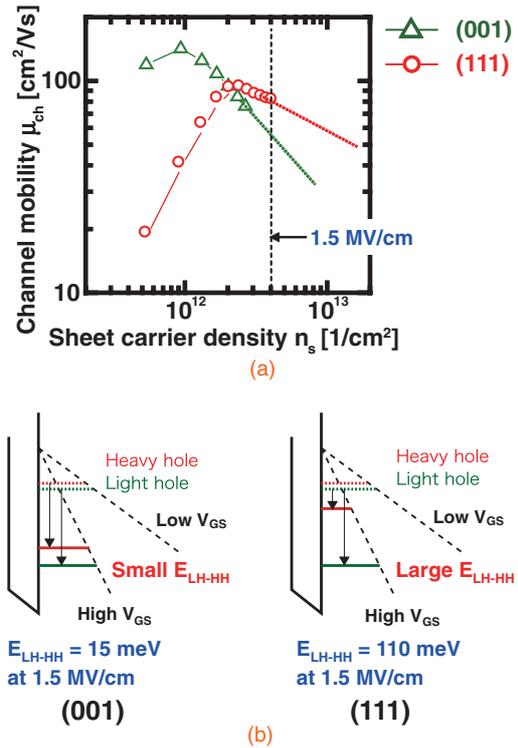


Fig. 3. (a) Sheet carrier concentration dependence of channel mobility on (001) and (111) diamond surfaces. (b) Schematics of subband structures in valence bands of diamond MOSFETs on (111) and (001) surfaces. The (111) surface shows large subband energy splitting owing to the large effective mass difference between heavy and light holes.

For submicron-gate-length diamond FETs, parasitic resistances R_S and R_D are not negligible in the total resistance between the source and drain terminals. Because of the parasitic resistances R_S and R_D , the effective gate-source voltage (V_{GS}') and effective drain-source voltage (V_{DS}') applied in the intrinsic region of submicron FETs are expressed as $V_{GS}' = V_{GS} - I_{DS}R_S$ and $V_{DS}' = V_{DS} - I_{DS}(R_S + R_D)$, respectively. Then, I_{DS} can be expressed as follows:

$$I_{DS} = \frac{W\mu_{\text{ch}}C_{\text{ox}}\left(V_{GS}' - V_{\text{th}} - \frac{V_{DS}'}{2}\right) \cdot V_{DS}'}{L}$$

$$= \frac{W\mu_{\text{ch}}C_{\text{ox}}\left(V_{GS} - V_{\text{th}} - \frac{V_{DS}}{2}\right) \cdot (V_{DS} - 2I_{DS}R_S)}{L}. \quad (1)$$

Here, W , L , μ_{ch} , and C_{ox} are the gate width, gate length, low-field channel mobility, and gate capacitance, respectively. Since the diamond MOSFETs were fabricated by the self-alignment gate lift-off technique, R_S is equal to R_D in the linear region of $I_{DS}-V_{DS}$ characteristics. Therefore, as shown in the bottom form of eq. (1), R_S can be substituted into R_D . Next, by summarizing I_{DS} on both sides of eq. (1), it can be rearranged as follows:

$$I_{DS} = \frac{W\mu_{\text{ch}}C_{\text{ox}}\left(V_{GS} - V_{\text{th}} - \frac{V_{DS}}{2}\right) \cdot V_{DS}}{L \left\{ 1 + 2 \left[\frac{W\mu_{\text{ch}}C_{\text{ox}}R_S\left(V_{GS} - V_{\text{th}} - \frac{V_{DS}}{2}\right)}{L} \right] \right\}}. \quad (2)$$

Equation (2) indicates that as R_S increases, the I_{DS} reduction becomes pronounced. The R_S is proportional to the sheet resistance of the hole accumulation layer. As shown in Fig. 1(a), the (111) diamond surface shows the lower sheet resistance than the (001) surface because the hole carrier density on the (111) surface is higher than that on the (001) surface. Therefore, the high I_{DS} on the (111) diamond surface is attributed to the low R_S owing to the low sheet resistance of the hole accumulation layer.

As shown in eq. (2), I_{DS} is also strongly affected by μ_{ch} , which is generally dependent on n_s . Then, μ_{ch} on the (111) and (001) surfaces at room temperature were evaluated to discuss the high I_{DSmax} on the (111) diamond surface. Figure 3(a) shows the n_s dependence of μ_{ch} for diamond MOSFETs. In the low n_s region, μ_{ch} increases with n_s . In addition, μ_{ch} decreases with n_s in the high n_s region. This tendency is similar to that of Si MOSFETs. Above the n_s of $3 \times 10^{12} \text{ cm}^{-2}$, μ_{ch} reduction on the (111) surface is more moderate than that on the (001) surface. While the (001) surface shows higher μ_{ch} below n_s of $3 \times 10^{12} \text{ cm}^{-2}$, μ_{ch} on the (111) surface is higher than that on the (001) surface in the high n_s region over $3 \times 10^{12} \text{ cm}^{-2}$. I_{DSmax} is determined by the sheet resistance under the gate electrode in the high n_s region, and the sheet resistance is inversely proportional to μ_{ch} and n_s . Therefore, in addition to the low R_S , higher μ_{ch} in the high n_s region contributes to the high I_{DSmax} on the (111) diamond surface.

In MOSFETs using two dimensional carrier channel, μ_{ch} in the high n_s region is mainly affected by the phonon and surface roughness scattering. Since the surface roughness of the (111) surface (RMS: $\sim 0.7 \text{ nm}$) is almost the same as that of the (001) surface (RMS: $\sim 0.5 \text{ nm}$) in diamond MOSFETs, μ_{ch} in the high n_s region is attributed to the difference in the phonon scattering in the (111) and (001) diamond films. Therefore, we evaluated the influence of the phonon scattering on μ_{ch} based on the subband structures of the hole accumulation layer on the (111) and (001) surfaces. On the H-terminated diamond surface, the energy band near the surface bends upward and hole carriers spontaneously accumulate near the surface.^{9,10} Most of the hole carriers exist within 10 nm from the surface¹¹ and therefore, the hole accumulation layer is composed of the several subband states due to carrier confinement effect.¹² The energy levels (ε_{sub}) of the subband states are determined by the hole effective mass with the direction perpendicular to the surface (m_{\perp}) which depends on surface orientation.

To investigate their subband structures, we calculated the first subband energies of heavy holes (HH) and light holes (LH) at the high n_s of $4 \times 10^{12} \text{ cm}^{-2}$. As a first-order approximation, we used a triangular potential well and an Airy function. The electric field strength (F) in the triangular potential well is determined from n_s [eq. (3)]. On the other hand, ε_{sub} is determined from m_{\perp} and F [eq. (4)].

$$F = \frac{e \cdot n_s}{\varepsilon_0 \cdot \varepsilon_{\text{diamond}}}, \quad (3)$$

$$\varepsilon_{sub} = 2.338 \times \left[\frac{(e \cdot F \cdot \hbar)^2}{2 \cdot m_0 \cdot m_{\perp}} \right]^{1/3}. \quad (4)$$

Here, e , \hbar , m_0 , ε_0 , and $\varepsilon_{\text{diamond}}$ are the elementary charge, Planck constant, electron mass, electric constant in a vacuum, and dielectric constant in diamond, respectively. The n_s of $4 \times 10^{12} \text{ cm}^{-2}$ corresponds to F of approximately 1.5

MV/cm, as shown in Fig. 3(a). Whereas m_{\perp} of the (111)-surface heavy hole (0.78) is much heavier than that of the (001)-surface heavy hole (0.43), m_{\perp} of the (111)-surface light hole (0.26) is lighter than that of the (001)-surface light hole (0.37).¹³ Figure 3(b) shows the schematics of subband structures in valence bands of diamond MOSFETs on (111) and (001) surfaces under high F of approximately 1.5 MV/cm. Because the (111) surface shows the greater difference in m_{\perp} of heavy and light holes than does the (001) surface, energy splitting between the first subband energies of the heavy and light holes (E_{LH-HH}) of the (111) surface (110 meV) is larger than that of the (001) surface (15 meV). In diamond films, the energy of a transverse acoustic phonon (E_{TA}) is $\sim 90 \text{ meV}$.¹⁴ As a result, in the high n_s region, E_{LH-HH} of the (111) surface is larger than E_{TA} , whereas E_{LH-HH} of the (001) surface is smaller than E_{TA} . Therefore, on the (111) surface, carrier scattering by phonon absorption between each subband (inter-subband scattering) could be reduced, and then, in the high n_s region, μ_{ch} on the (111) surface decreases more gradually than that on the (001) surface and higher μ_{ch} is obtained on the (111) surface.

Because of the high H-C dipole charge density on H-terminated (111) diamond surface, the (111) surface shows higher hole carrier density than the (001) surface. For diamond MOSFETs on the (111) surface, I_{DSmax} of -850 mA/mm was obtained. This I_{DSmax} value is the highest reported to date for diamond FETs and is due to the reduction of R_S and R_D and the high μ_{ch} at high V_{GS} . The reduction of R_S and R_D is a result of the low sheet resistance on the (111) diamond surface. On the other hand, the high μ_{ch} at high V_{GS} on the (111) diamond surfaces is attributable to the reduction of inter-subband scattering between LH and HH because the E_{LH-HH} is greater than the E_{TA} .

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