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AlGaN/GaN/AlGaN Double Heterostructures Grown on 200 mm Silicon (111) Substrates with High Electron Mobility

Kai Cheng, Hu Liang, Marleen Van Hove, Karen Geens, Brice De Jaeger, Puneet Srivastava, Xuanwu Kang, Paola Favia, Hugo Bender, Stefaan Decoutere, Johan Dekoster, Jose Ignacio del Agua Borniquel[1], Sung Won Jun[2], and Hua Chung[2]

IMEC, Kapeldreef 75, B-3001 Leuven, Belgium
[1]*Applied Materials, Kapeldreef 75, B-3001 Leuven, Belgium*
[2]*Applied Materials, 3050 Bowers Ave, Santa Clara, CA 95054-3201, U.S.A.*

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In this work, we demonstrate, for the first time, $Al_{0.35}GaN/GaN/Al_{0.25}GaN$ double heterostructure field effect transistors on 200 mm Si(111) substrates. Thick crack-free $Al_{0.25}GaN$ buffer layers are achieved by optimizing $Al_{0.75}GaN/Al_{0.5}GaN$ intermediate layers and AlN nucleation layers. The highest buffer breakdown voltage reaches 1380 V on a sample with a total buffer thickness of 4.6 μm. According to Van der Pauw Hall measurements, the electron mobility is 1766 $cm^2\,V^{-1}\,s^{-1}$ and the electron density is $1.16 \times 10^{13}\,cm^{-2}$, which results in a very low sheet resistance of $306 \pm 8\,\Omega$/square. © 2012 The Japan Society of Applied Physics

GaN has been considered as the most important semiconductor next to silicon because of its applications in solid-state lighting and high power switching devices. Thanks to its high critical electric field of 3.5 MV/cm, GaN is a promising wide-band-gap material for next-generation power switching devices. Excellent GaN power devices that break the silicon limit have been demonstrated by different groups.[1–5] In order to reduce the manufacturing cost of GaN power devices, the GaN-on-Si approach has attracted more and more of industry's attention because silicon substrates are cheap, of high quality and available in large size. Recently, (Al)GaN layers grown on 150- and 200-mm silicon substrates have been reported.[6–10]

In our previous work, we demonstrated excellent high-electron-mobility transistors (HEMT) and double heterostructure field effect transistors (DH-FET) on 100- and 150-mm Si(111) substrates.[11,12] In this study, we show, for the first time, that it is feasible to grow crack-free AlGaN/GaN/AlGaN double heterostructures with thick AlGaN buffer layers on 200-mm Si(111) substrates by metal organic vapor phase epitaxy (MOVPE). As these wafers need to be processed in a complementary metal–oxide–semiconductor (CMOS) compatible fab, the wafer quality should meet strict CMOS process standards. For example, the wafer bow needs to be well controlled below ±50 μm in order to reduce failure during wafer handling and pass the stepper in the lithography process. In ref. 12, we showed that the radius of wafer curvature could reach 40 m with a single $Al_{0.45}GaN$ intermediate buffer layer. However, on a 200-mm wafer, the radius of wafer curvature needs to exceed 100 m in order to meet the wafer bow specification of 50 μm. Thus, it is crucial to fine tune the AlGaN intermediate layers and minimize the wafer bow. In addition to the buffer layer optimization, the active region is also investigated. We demonstrate that the sheet resistance of $Al_{0.35}GaN/GaN/Al_{0.25}GaN$ DH-FET is as low as $306 \pm 8\,\Omega/\square$. The electron mobility is 1766 $cm^2\,V^{-1}\,s^{-1}$ and the electron density is $1.16 \times 10^{13}/cm^2$ according to Van der Pauw Hall measurements.

$Al_{0.35}GaN/GaN/Al_{0.25}GaN$ double heterostructures are grown on 200-mm Si(111) substrates by MOVPE in a showerhead reactor from Applied Materials. Trimethylgallium, trimethylaluminum and ammonia are used as precursors for Ga, Al, and N, respectively. H_2 is used as carrier gas. First of all, an AlN nucleation layer (NL) is grown to prevent melt-back etching between Ga and Si and also to improve the wetting properties of III–nitrides on Si. The AlN NL is optimized in terms of both structural quality and surface morphology. On top of the AlN NL, $Al_{0.25}GaN$ buffer layers are grown with two $Al_{0.75}GaN$ and $Al_{0.5}GaN$ intermediate layers. Two series of samples have been grown to optimize the thicknesses of the $Al_{0.25}GaN$ buffer layer and the $Al_{0.75}GaN$ and $Al_{0.5}GaN$ intermediate layers in order to achieve a flat wafer. In the end, based on the optimized buffer structure, $Al_{0.35}GaN/GaN/Al_{0.25}GaN$ DH-FET is demonstrated. The GaN channel thickness is 150 nm and a 10-nm-thick $Al_{0.35}GaN$ layer is used as barrier layer. A 1-nm-thick Si_3N_4 layer is grown to stabilize and passivate the $Al_{0.35}GaN$ surface in DH-FET. The structural quality is evaluated by high-resolution X-ray diffraction (HR-XRD) and the microstructure is investigated by cross-sectional scanning transmission electron microscopy (S-TEM).

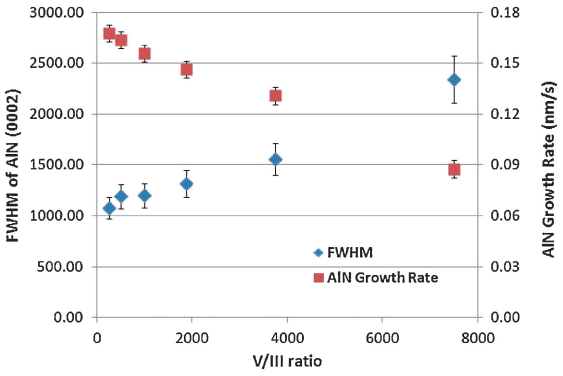

Fig. 1. Influence of V/III ratio on AlN growth rate and crystal quality.

First, the growth parameters of the AlN nucleation layer are investigated, including growth temperature, growth pressure, and V/III ratio. The AlN NL thickness is 220 nm. We find that the V/III ratio has a pronounced impact on both crystalline quality and surface morphology. By decreasing the V/III ratio from 7500 to 250, the growth rate of AlN is almost doubled, as shown in Fig. 1. The enhanced AlN growth rate at low V/III ratio is because of the suppressed gas phase reaction between TMAl and NH_3.[13] In the case of high ammonia flow, nanoparticles are generated resulting in undesired nuclei in the epi-layers and the deterioration of

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Table I. Overview of characterization results of Sample Series A and B.

No	$Al_{0.5}GaN/Al_{0.75}GaN$ thickness (nm)	$Al_{0.25}GaN$ thickness (nm)	Wafer bow (μm)	$Al_{0.25}GaN$ (002)	$Al_{0.25}GaN$ (102)
A1	200/200	970	67	777	1029
A2	200/200	1260	73	700	934
A3	200/200	1590	59	653	843
A4	200/200	1870	38	645	840
B1	400/400	1900	13	539	1020
B2	600/600	3170	−130.1	499	914

the crystal quality and surface morphology. In addition, the mobility of aluminum atoms is also limited under an NH_3-rich condition, which may roughen the surface. However, at a low V/III ratio, the gas phase reaction is minimized.[13] Thus, both crystal quality and surface morphology are improved significantly when the V/III ratio is below 1000. The surface morphology is analyzed by tapping mode AFM, and the root mean square (rms) roughness is as low as 0.5 nm in a scan area of $5 \times 5\,\mu m^2$. The crystalline quality is evaluated by HR-XRD rocking curve symmetric (0002) ω-scan, as shown in Fig. 1. The full width at half-maximum (FWHM) of the AlN(0002) ω-scan is around 1200 arcsec when the V/III ratio is below 1000, which is among the best values reported in the literature.[14,15]

In previous work,[16] we showed that it is feasible to grow thick (~2.3 μm) crack-free unintentionally doped GaN (u-GaN) on 200-mm Si by introducing a 200-nm-thick $Al_{0.5}GaN$ intermediate layer. The single $Al_{0.5}GaN$ intermediate layer can introduce sufficient compressive stress to the top u-GaN layer and thus counterbalances the thermal tensile stress in the nitride layers imposed by the silicon substrates. In the sample with 2.3-μm-thick u-GaN, the wafer bow was still below 20 μm. In accordance with this experience obtained in u-GaN growth, we decide to introduce another $Al_{0.75}GaN$ intermediate layer of 200 nm between the AlN NL and the $Al_{0.5}GaN$ layer for stress management. By using the $Al_{0.75}GaN/Al_{0.5}GaN$ bi-layer, it is feasible to grow the thick (>1 μm) $Al_{0.25}GaN$ buffer layers, which is required to achieve high breakdown voltage in $Al_{0.35}GaNs/GaN/Al_{0.25}GaN$ DH-FETs on Si. Two series of samples have been grown to address the bow issues.

In the first series of four samples A1–A4, the $Al_{0.25}GaN$ buffer thickness is varied from 0.97 to 1.87 μm. The layer stack information, and characterization results are summarized in Table I. All the samples are crack-free and mirror-like, as evidenced by optical microscope inspection. The wafer bow is measured by a laser profilometer in two perpendicular directions, and all samples show convex wafer bow at room temperature. The $Al_{0.75}GaN/Al_{0.5}GaN$ intermediate bi-layer is very efficient to supply compressive stress to the $Al_{0.25}GaN$ buffer. It is worth noting that the maximum convex wafer bow is reached at the $Al_{0.25}GaN$ thickness of 1.26 μm. The incremental stress is still compressive even after 1-μm-thick $Al_{0.25}GaN$ growth. However, when the $Al_{0.25}GaN$ layer thickness reaches 1.59 μm, the convex wafer bow decreases from 74 to 37 μm because the compressive stress is relaxed and is not longer sufficient to compensate the thermal tensile stress. *In situ* curvature measurements by EpiCurve TwinTT from Laytec also

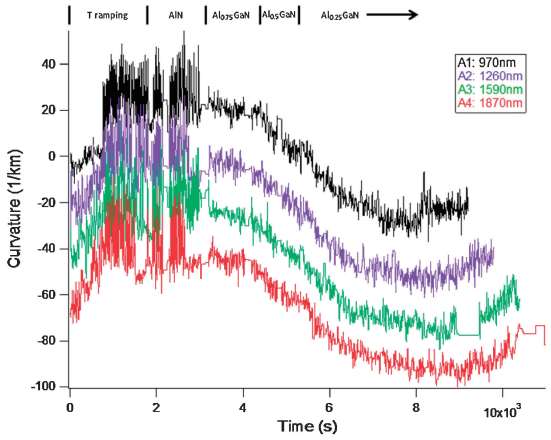

Fig. 2. *In situ* curvature measurements of Samples A1–A4. *In situ* monitoring system stops working when the wafer is taken out of the growth chamber at 500 °C.

confirm that the incremental compressive stress is completely relaxed when the $Al_{0.25}GaN$ layer is thicker than 1.26 μm, as shown in Fig. 2. As is observed by *in situ* curvature measurements, the silicon wafers already show certain wafer bow during ramping up of the temperature owing to the thermal gradient in the substrate. The growth stress in AlN and $Al_{0.75}GaN$ is negligible as the curvature does not change during AlN and $Al_{0.75}GaN$ growth. During $Al_{0.5}GaN$ and $Al_{0.25}GaN$ growth however, significant compressive stress is introduced. The average growth stresses of $Al_{0.5}GaN$ and $Al_{0.25}GaN$ in Sample A2 are 2.7 and 0.8 G Pa, respectively, if we assume that the biaxial modulus of Si wafers at the growth temperature is still 203 G Pa.[17] In Samples A3 and A4, the average growth stress of $Al_{0.25}GaN$ layers is 0.64 and 0.54 G Pa, respectively. The average stress decreases because the growth stress is completely relaxed when the $Al_{0.25}GaN$ layer thickness exceeds 1.26 μm.

The structural quality of the $Al_{0.25}GaN$ buffer layers has been characterized by HR-XRD, as shown in Table I. By increasing the $Al_{0.25}GaN$ buffer thickness, the crystalline quality can be significantly improved. In the best sample, the FWHM of the symmetric (0002) and asymmetric ($\bar{1}102$) ω-scan are 645 and 840 arcsec, respectively. These values are comparable to the previous ones obtained on 4-in. silicon substrates[11] and the best values in the literature.[18–20]

In the second series of samples, the thickness of the $Al_{0.75}GaN/Al_{0.5}GaN$ intermediate bi-layer is increased from 200 nm for each layer to 400 nm in Sample B1 and 600 nm in Sample B2. The sample information and characterization results have been summarized in Table I. The $Al_{0.25}GaN$ buffer thicknesses in Sample B1 and Sample B2 are 1.87 and 3.2 μm, respectively. In addition, a 150-nm-thick GaN layer is added in order to check the surface morphology of the GaN channel in the DH structure. These two samples are both mirror-like and crack-free, as shown in Fig. 3(a). The wafer bow of Sample B1 is below 20 μm, but Sample B2 shows large concave wafer bow of 130 μm. The surface morphology of Sample B1 has been analyzed by tapping mode AFM, as shown in Fig. 3(b). The rms roughness is 0.3 nm in a $2 \times 2\,\mu m^2$ scan area. The threading dislocation density is estimated to be $(6–8) \times 10^9\,cm^{-2}$. The smooth

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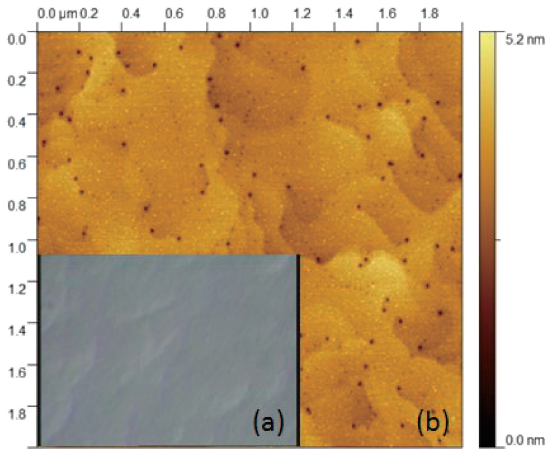

Fig. 3. (a) Optical microscope inspection shows the crack-free surface of Sample B2. (b) Surface morphology of Sample B1 as evaluated by tapping mode AFM.

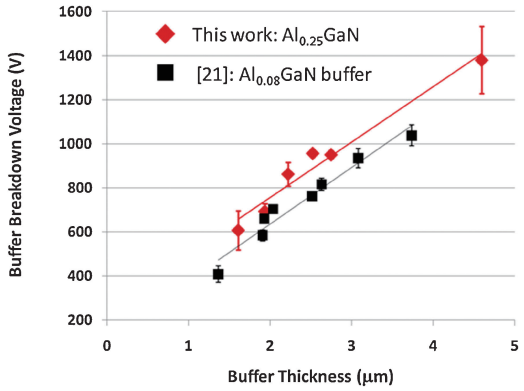

Fig. 4. Buffer breakdown voltage versus the total layer thickness.

surface is beneficial for achieving high electron mobility because of minor interface scattering.

Besides the structural quality, the breakdown voltage of these two series of samples has been measured as well. Ti/Al/Ti/TiN based ohmic contacts are isolated by mesa etching with a gap of 32 µm. The breakdown measurements are carried out with the samples immersed in an inert liquid (Fluorinert FC-77) to prevent surface flash over with the substrates floating. We define the breakdown voltage as the value at which the leakage current between ohmic contacts of the isolation structures increases to 1 mA/mm. The breakdown behaviour versus total buffer thickness is shown in Fig. 4. The buffer breakdown voltage improves linearly with increasing total buffer thickness. Sample B2 with the thickest buffer shows the highest breakdown voltage of 1380 V. The data obtained in this work are also benchmarked with the earlier published results obtained on 4-in. Si substrates.[21] Thanks to the higher aluminium composition of the buffer layers used in the current work, the breakdown voltage is slightly higher when the same buffer layer thickness is used.

Sample B1 shows very good buffer breakdown of >950 V. Moreover, the wafer bow of B1 is well below 20 µm, which is essential in processing these wafers in a CMOS-compatible fab. Thus, the DH-FET device structures were grown on the optimized buffer layer of Sample B1. From the top to the bottom, the active region consists

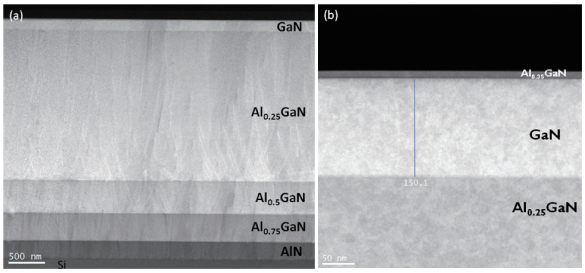

Fig. 5. Cross-sectional scanning TEM of (a) the whole layer stack and (b) the active region.

of 4 layers: 1 nm *in situ* SiN, a 10 nm $Al_{0.35}GaN$ barrier, a 150 nm GaN channel, and a 1.87 µm $Al_{0.25}GaN$ buffer. The whole epi layer stack has been characterized by cross-sectional scanning TEM, as shown in Fig. 5. All the interfaces are sharp, the AlN nucleation layer is smooth, and there are no reversed pyramids present. Thanks to the *in situ* SiN passivation layer, the $Al_{0.35}GaN$ barrier layer is also smooth and no pits are visible.[22]

The electrical properties of $Al_{0.35}GaN/GaN/Al_{0.25}GaN$ DH-FET are characterized by Van der Pauw Hall measurements. Five points are measured from the wafer center to the edge. The average electron mobility is 1766 ± 19 $cm^2\,V^{-1}\,s^{-1}$ and the electron density is $(1.16 \pm 0.02) \times 10^{13}\,cm^{-2}$, which results in a very low sheet resistance of $306 \pm 8\,\Omega/\square$. These values even outperform the ones obtained on 150-mm silicon substrates.[12] The processed devices show a current density of 0.65 A/mm. More detailed device results will be published elsewhere.

In conclusion, we have shown the feasibility of growing high quality AlGaN/GaN/AlGaN DH-FETs on a 200-mm Silicon platform. By optimizing the AlN nucleation layer and the $Al_{0.75}GaN/Al_{0.5}GaN$ intermediate layers, the wafer bow is controlled to less than 20 µm, which enables device processing in a CMOS-compatible fab. The electron mobility is as high as $1766\,cm^2\,V^{-1}\,s^{-1}$ and the electron density is $1.16 \times 10^{13}\,cm^{-2}$. GaN-based power devices grown on 200-mm Si substrates show great potential for integrating GaN processing on a standard silicon technology platform.

1) Y. Uemoto *et al.*: IEDM Tech. Dig., 2007, p. 861.
2) Y. Wu *et al.*: IEEE Electron Device Lett. **29** (2008) 824.
3) N. Ikeda *et al.*: Proc. IEEE **98** (2010) 1151.
4) S. Iwakami *et al.*: Jpn. J. Appl. Phys. **46** (2007) L587.
5) Y. Dora *et al.*: IEEE Electron Device Lett. **27** (2006) 713.
6) A. Ubukata *et al.*: J. Cryst. Growth **298** (2007) 198.
7) A. Boyd *et al.*: Phys. Status Solidi C **6** (2009) s1045.
8) A. Dadgar *et al.*: J. Cryst. Growth **297** (2006) 279.
9) J. Li *et al.*: Appl. Phys. Lett. **88** (2006) 171909.
10) D. Zhu *et al.*: Proc. SPIE **7231** (2009) 723118.
11) Kai Cheng *et al.*: Phys. Status Solidi C **5** (2008) 1600.
12) Kai Cheng *et al.*: Jpn. J. Appl. Phys. **47** (2008) 1553.
13) A. V. Lobanova *et al.*: J. Cryst. Growth **287** (2006) 601.
14) H. P. D. Schenk *et al.*: J. Cryst. Growth **200** (1999) 45.
15) I. Gherasoiu *et al.*: J. Appl. Phys. **96** (2004) 6272.
16) Kai Cheng *et al.*: LED Prof. **26** (2011) 28.
17) S. P. Nikanorov *et al.*: Sov. Phys. Solid State **13** (1971) 2516.
18) H. Ishikawa *et al.*: Phys. Status Solidi C **0** (2003) 2177.
19) S. Arulkumaran *et al.*: Appl. Phys. Lett. **86** (2005) 123503.
20) P. Saengkaew *et al.*: J. Cryst. Growth **311** (2009) 3742.
21) D. Visalli *et al.*: Jpn. J. Appl. Phys. **48** (2009) 04C101.
22) J. Derluyn *et al.*: J. Appl. Phys. **98** (2005) 054501.

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